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Voltage Overstress Protection in CMOS ICs

Continuing technological shrinkage brings to lowering possible maximum voltages applied to MOS devices and IC supply voltages. High voltages applied to CMOS devices bring to devices' failures or parametrical degradation during the time. Main physical phenomenon resulting in MOS degradation/failure because of voltage overstress: HCI – Hot Carrier Injection; NBTI – Negative Bias Temperature Instability; TDDB – Time Dependent Dielectric Breakdown; SILC – Stress Induced Leakage Current. Device performance time can be increased either by improving technological processes or using newer approaches in circuit designs. **(Slide 3)**.

The table **(Slide 4)** represents the typical gate oxide thickness and supply voltages depending on technological processes. For 32nm processes there is an adverse effect in thickness change caused by use of dielectrics with higher dielectric constants. Usually max allowed voltage over MOS two different nodes is VDD+20%.

There is a lot of IO standards nowadays which still use 3.3V as one of supplies (USB, PCI, etc.). Most susceptible blocks to overstress in these designs are: level shifters and IO cells. Benefits of using low voltage device are: gain in area/performance, which results in cost/power, and there is no need in additional mask, which affects on cost. The drawback is reliability issues under high voltage operation. **(Slide 5)**.

Schematic of Conventional level-shifter presented (**Slide 6**), which will break-down if it will be based on 2.5V or 1.8V devices.

USB FS(Full-Speed) driver's conventional architecture presented, and devices which will have reliability issues in case if they will be implemented on 2.5V or 1.8V devices (**Slide 7**).

One of proposed approaches for overstress protection: cascading (**Slide 8**). Cascoding allows redistributing large voltage over several series connected devices but costs area/ performance.

Voltage limitation circuit represented (**Slide 9**). V(OUT) chooses highest from two inputs.

Proposed level-shifter's schematic implemented on 1.8V devices with cascading technique implemented (**Slides 10, 11**). Circuit provides two invert outputs Q and QN with: V_{LO}=VDD18, VHI=VDD33. Additional cross coupling improves performance and relieves overstress.

Dual output level-shifter represented with outputs in 1.8V and 3.3V domains (**Slide 12**).

Proposed USB Full-Speed driver's schematic, where cascading employed for overstress reduction, during 3.3V signaling. (**Slide 13**). The solution is for 2.5V devices.

Proposed USB Full-Speed driver's schematic, where cascading employed for overstress reduction, during 3.3V signaling, as well as voltage limitation circuit for proper biasing of upper cascade device. (**Slide 14**). The solution is for 1.8V devices.

Lifetime calculation methodology presented, where overstress voltage, lifetime under DC overstress, overstress duration are incorporated in equation (**Slide 15**). The calculation is pessimistic as it incorporates highest voltage.

Conclusion. (**Slide 16**) Cascoding as a method of voltage distribution over several devices is proposed. Voltage limitation circuit for preventing from wide voltage swing is proposed. USB FS driver configuration and level-shifter design based on 1.8V devices with lifetime more than 10yrs are proposed. Lifetime calculation methodology proposed. Level-shifter and USB FS driver designs are silicon proven.