“REGULARITIES OF POWER CONSUMPTION IN QUASIADIABATIC LOGIC GATES”

2nd slide

On the first slide you can see power density trend. As one can see power density is essentially increasing during scaling.

3rd slide

One of the most important problem in modern microelectronics is the reduction of power consumption in digital devices of information processing.

4th slide

Average power consists of switching power, short-circuit power and leakage power. Among traditional ways to reduce power consumption there are algoritmical, logical, topology and technology ways. There are several ways to reduce active power. We can reduce switched capacitance by minimizing loading from diffusion, wire and gate or by using more efficient layout techniques. We can reduce dynamic voltage and supply voltage by technology scaling. We also can try to reduce switching activity by means of conditional execution, conditional clocking, conditional precharge and turn off the blocks which are not active. Another way is reduction of clock frequency.

5th slide

The radical method of reducing the power consumption consists in use of a principle of thermodynamic reversibility. It may be achieved by applying of the controlled power supply. At the activation stage the gate carries out logic operations with consuming of energy. At the deactivation stage the energy which has been saved up in reactive elements, comes back in the power supply.
The maximal reduction of power consumption is reached in quasiadiabatic gates.

Traditional CMOS gates with one phase power supply can work in quasiadiabatic stage (1n1p- logic). 1n1p gates circuit, timetable of Vi voltage at i-gate output and supply voltage are shown at the picture VQ-diagrams which show dependence of accumulated in output capacitance charge from supply voltage are convenient ways to analyse energy loss. Energy is thermalized during one switch of the gate is equal (see picture 1.6в) the square of the curve. If supply voltage is changing slowly energy is thermalized only when transistors start to open, voltages on capacitances are changed stepwise and accumulated charge is drained through the channel resistances. The main disadvantage of 1n1p- logic is that it can't work in pipelining. To work in pipelining gate need internal storage to store information when voltage is taken from the previous gate.

6th slide

It is realized in Denker's logic with four-phase power supply. Short circuit current is absent due to use of direct and reverse signals. It provides that one of the load p-channel transistors will be closed. P-channel transistors gates are not connected with gate inputs so taking supply voltage from the previous cascade is not cause there to open. You can see the work of 2n-2n2p inverter at timetable picture . During the activation phase 1 supply voltage of i-gate is increasing from zero to supply voltage and it is taking input information forming the signals on direct and inverse outputs. During storage phase 2 supply voltage of previous (i-1)–gate is taken off but information from i-gate is storing in trigger and is taking by (i+1)-gate which is an activation phase. During phase 3 i-gate is deactivated with returning stored energy back to supply voltage and after phase 4 when (i-1)-gate is activated i-gate is ready to take the new information from it. As you can see on the timetable when gradient of supply voltage is infinite small energy dissipation occurs only when gate's logical level is changing and its

output capacitance voltage is changing stepwise. The main disadvantage of 2n-2n2p-gate is necessity to use both the direct and inversion signals what doubles the amount of signal buses and thermalized energy.

7th slide

The main characteristics of static quasiadiabatic gates are shown in the table .
Основные характеристики квазиадиабатических вентилей статического типа сведены в таблице.

8th slide

In dynamic quasiadiabatic logic the output electrodes in some time periods don't have galvanic connections with supply voltage buses. At that one of the voltage logical levels is stored on output electrode capacitance. In ECRL-logic (Efficient Charge Recovery Logic) capacitances which keep information are charged not by rectifying elements but by p-channel transistors together with generating the output signals. It can be reached by using both the direct and inversion logical signals. ECRL use gates with four-phase power supply. Inverter logic circuit and timetables of working impulses are shown on the picture . VQ-diagrams on the picture show that transitions without changing logical state (0-0, 1-1) are not dissipative but during cyclic transitions each of two gate capacitances is recharged with energy thermalization.

9th ,10th slides

Power characteristics of quasiadiabatic gates were researched with Spectra program from CADENCE CAD Tools.
The effect of abnormal high power consumption in a range of low frequencies was discovered. It is shown that this effect is associated with short circuit current at change of a logic condition and the method of its neutralization is offered. It is revealed that energy dissipation in gates decreases in a range of high frequencies at the reduction of clock frequency more poorly than under the 1/f law.
The dependencies of power dissipation for base logic gates are established and numerical values of parameters describing them are found.