UNIVERSAL ASYNCHRONOUS RECEIVER / TRANSMITTER (UART)

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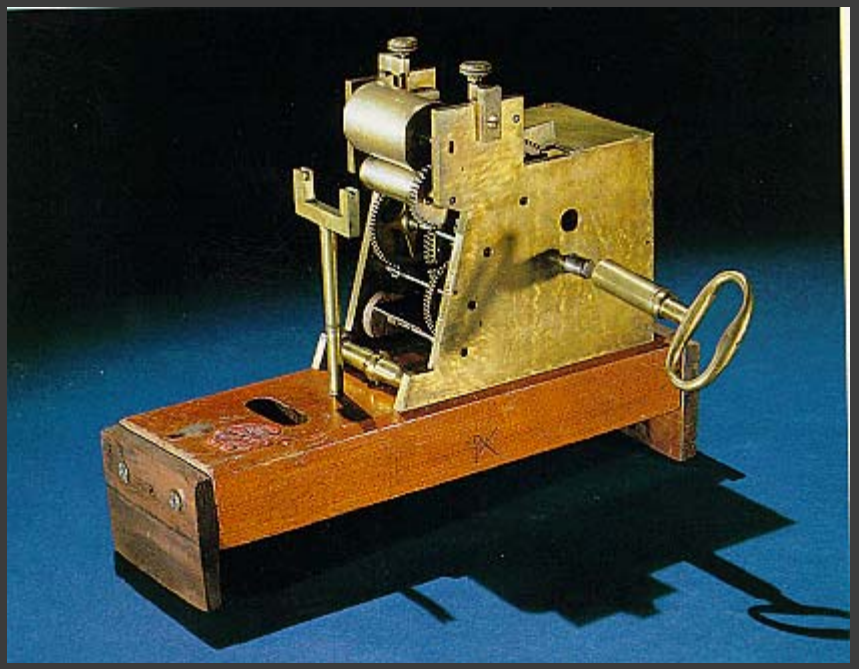
History of UART - telegraph

The first UART-like devices (with fixed-length pulses) were rotating mechanical switches (commutators). These sent 5-bit Baudot codes for mechanical teletypewriters, and replaced morse code. Later, ASCII required a seven bit code. When IBM built computers in the early 1960s with 8-bit characters, it became customary to store the ASCII code in 8 bits.

The first receiver



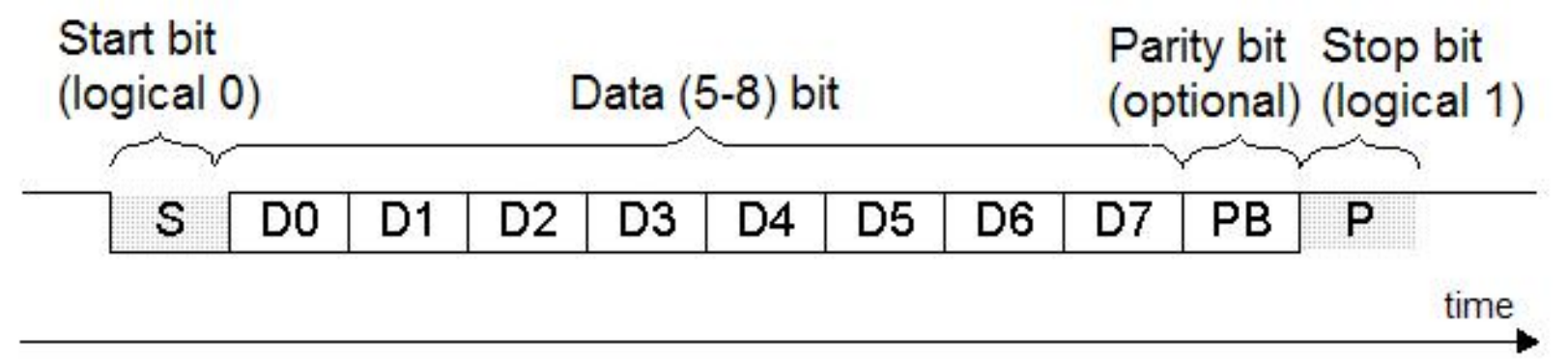
Telegraph Register Patent Model, patented May 1, 1849, patent number 6,420, by Samuel F. B.Morse

UART controller nowadays

Orient XWT-PS050

Serial interface controller, based on 16C550 UART standard

FRAME STRUCTURE



Data frame consists of:

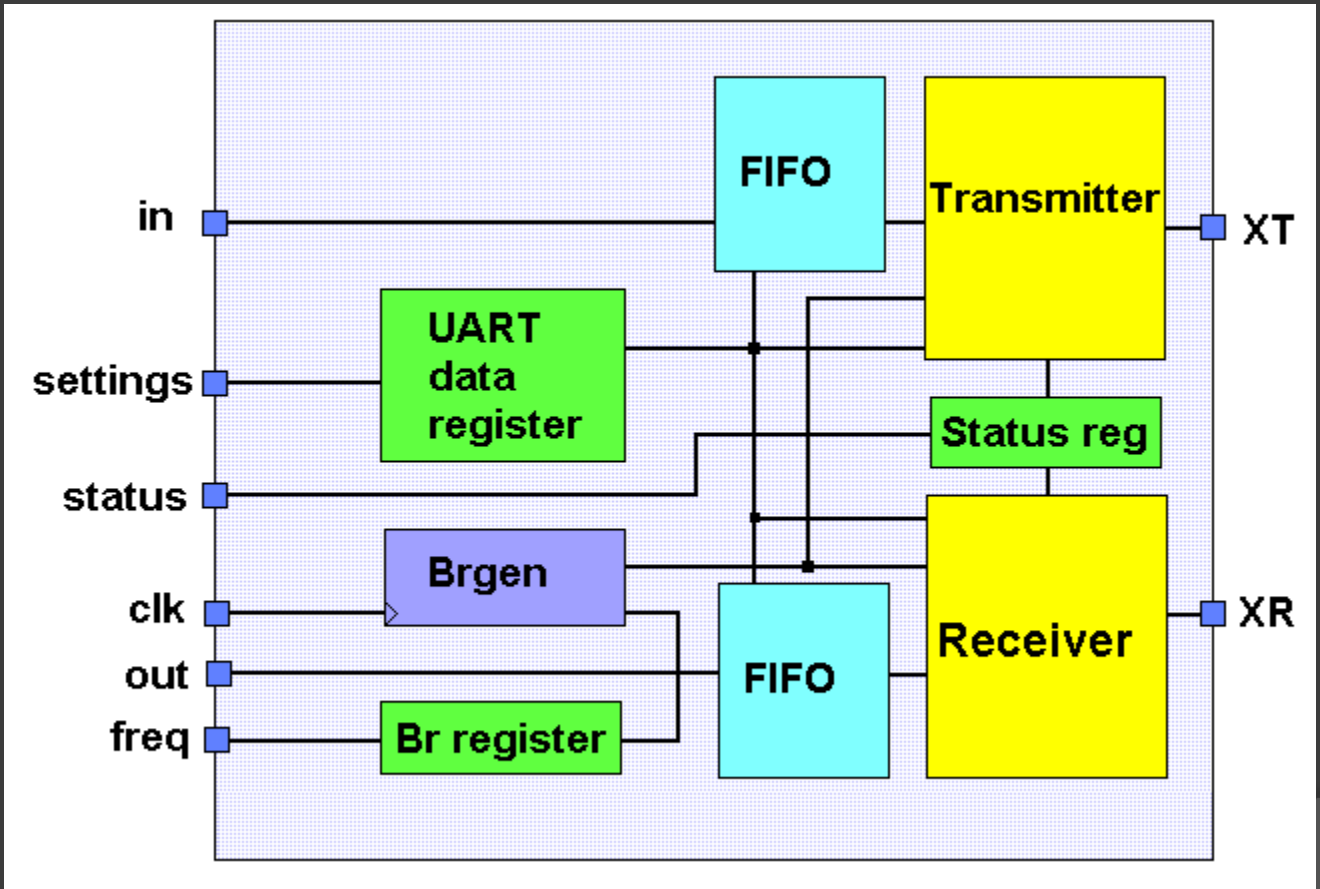
- Start bit
- 5-8 data bits
- Parity bit(optional)
- Stop bit

UART STRUCTURE

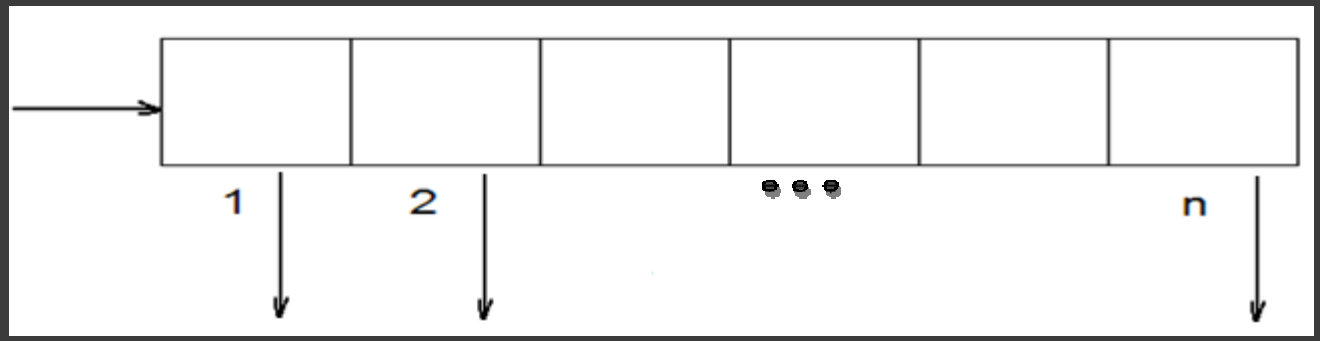
A UART usually contains the following components:

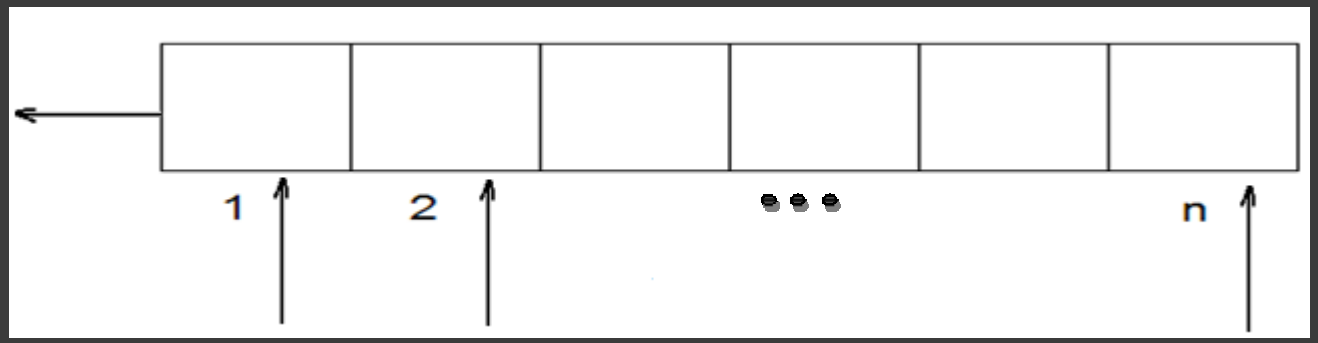
- a clock generator
- input and output shift registers
- transmit/receive control logic
- read/write control logic
- First-in, first-out (FIFO) buffer memory (optional)

UART STRUCTURE



Serial to parallel algorithm





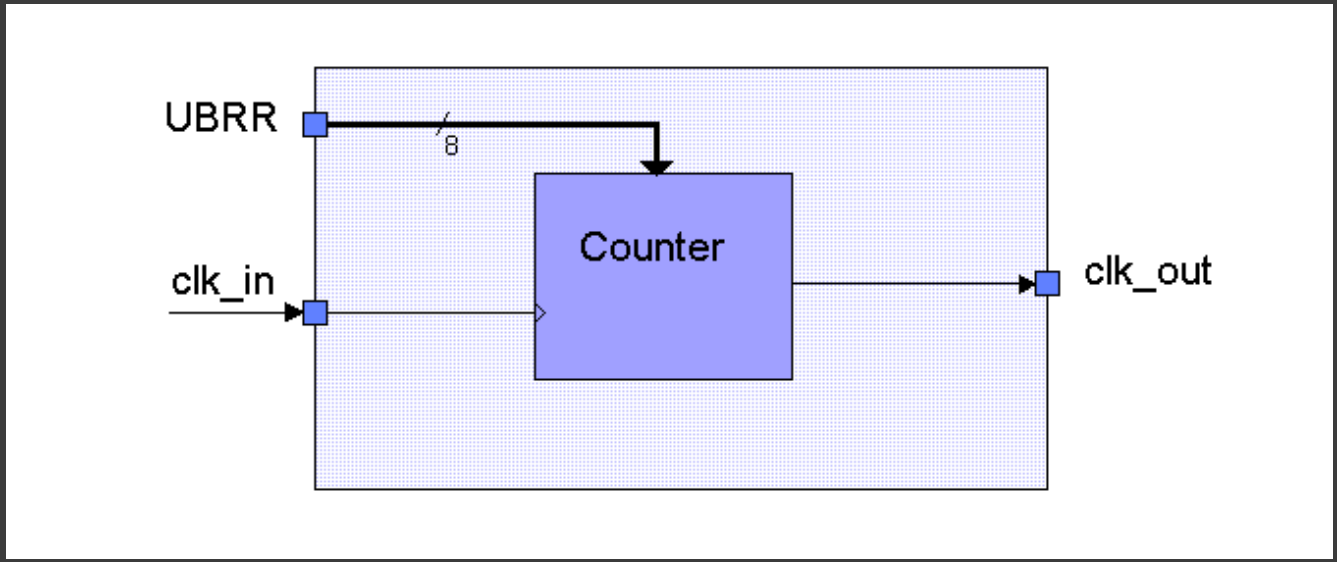
UART is based on shift register. There 2 registers – one in receiver and one in transmitter

Baud rate generator

As UART works with external line, it function slower than CPU.

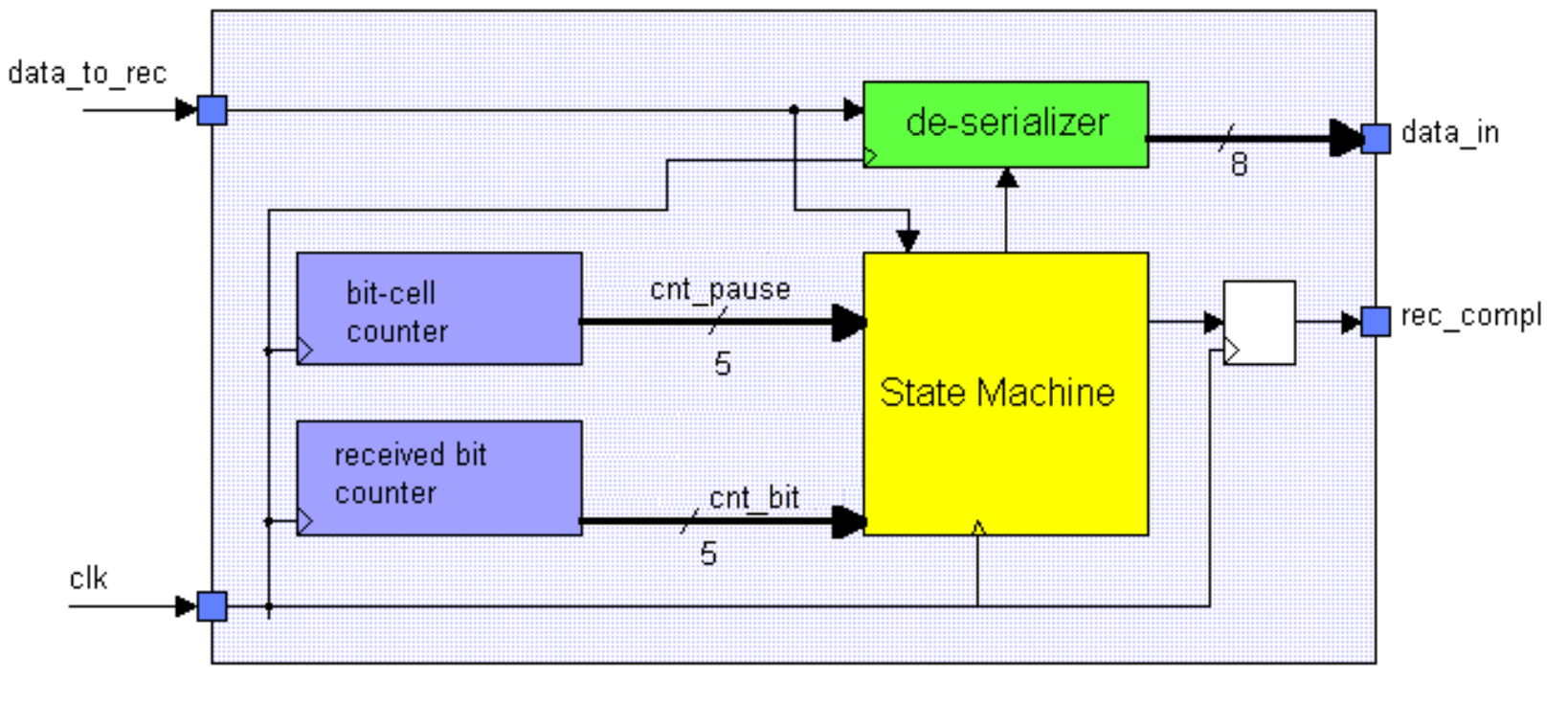
All operations of the UART hardware are controlled by a clock signal which runs at a multiple (say, 16) of the data rate - each data bit is as long as 16 clock pulses.

Baud rate generator structure



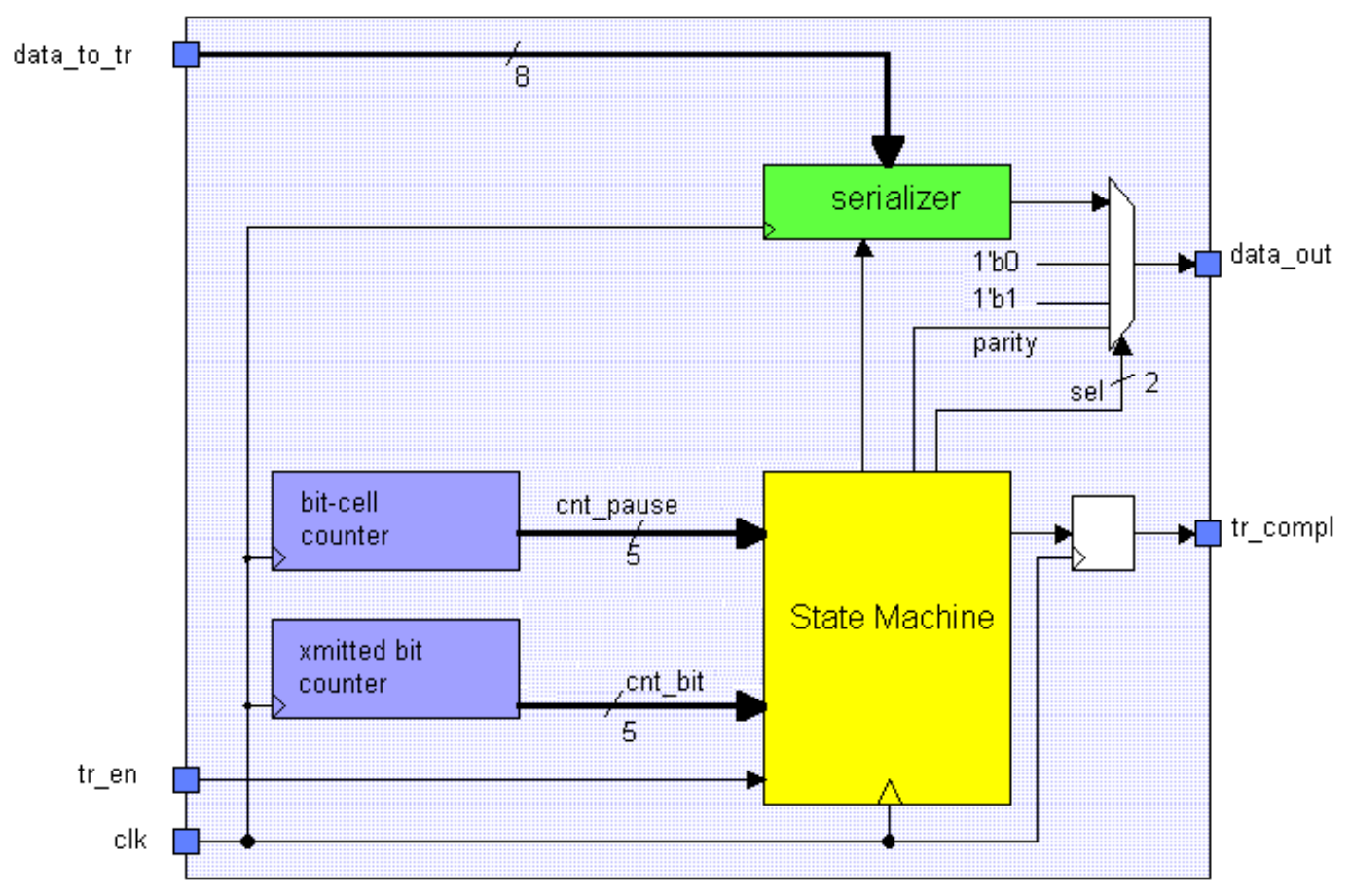
Baud rate generator is used for setting internal clock frequency and for changing transfer rate of UART.

RECEIVER STRUCTURE



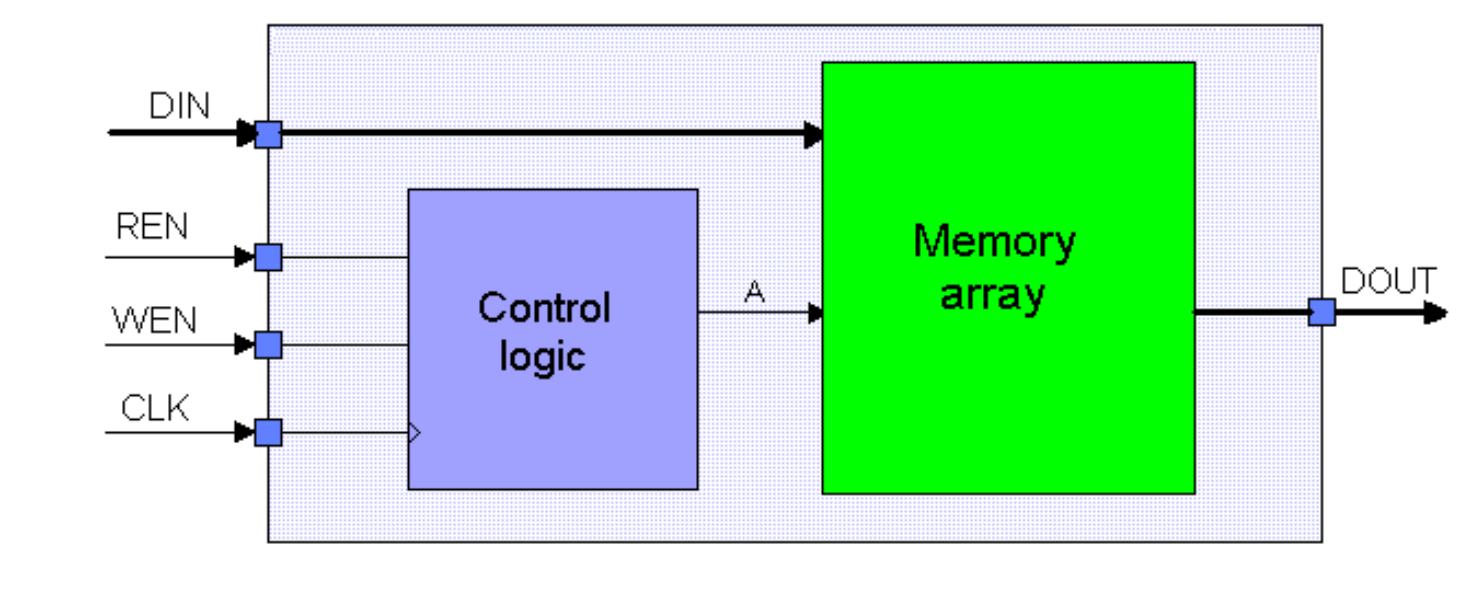
Receiver is used for receiving data from 1 bit input and to transform this data to 8 bit output.

Transmitter structure



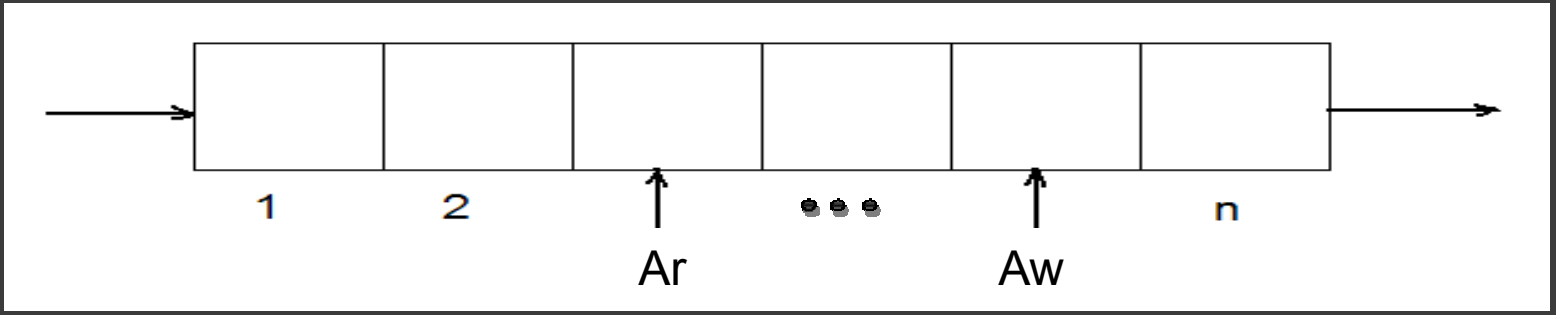
Transmitter is used to shift 8 bit data bit by bit to data bus.

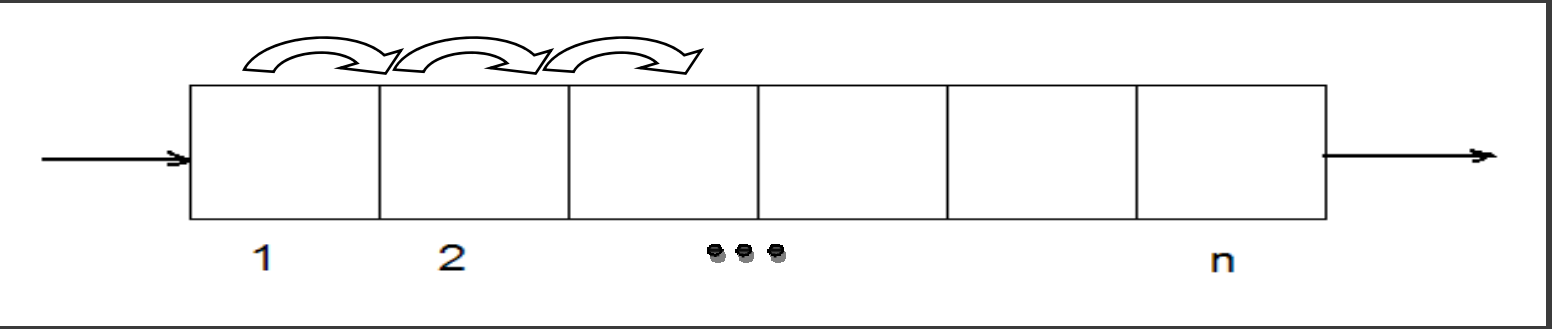
FIFO buffers structure



There are 2 buffers in UART. One is used for gathering data for receiver and one for transmitter. Receiver buffer saves data received from bus to make it accessible any time. Transmitter buffer gathers data to be transmitted.

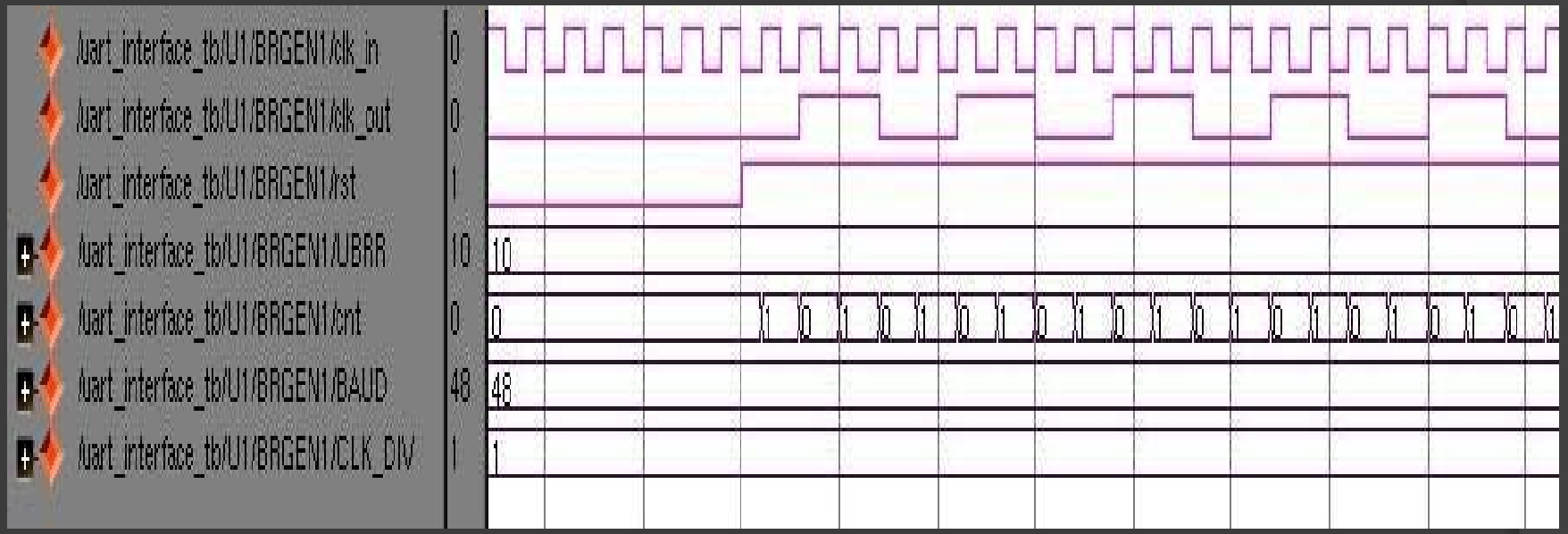
FIFO buffer





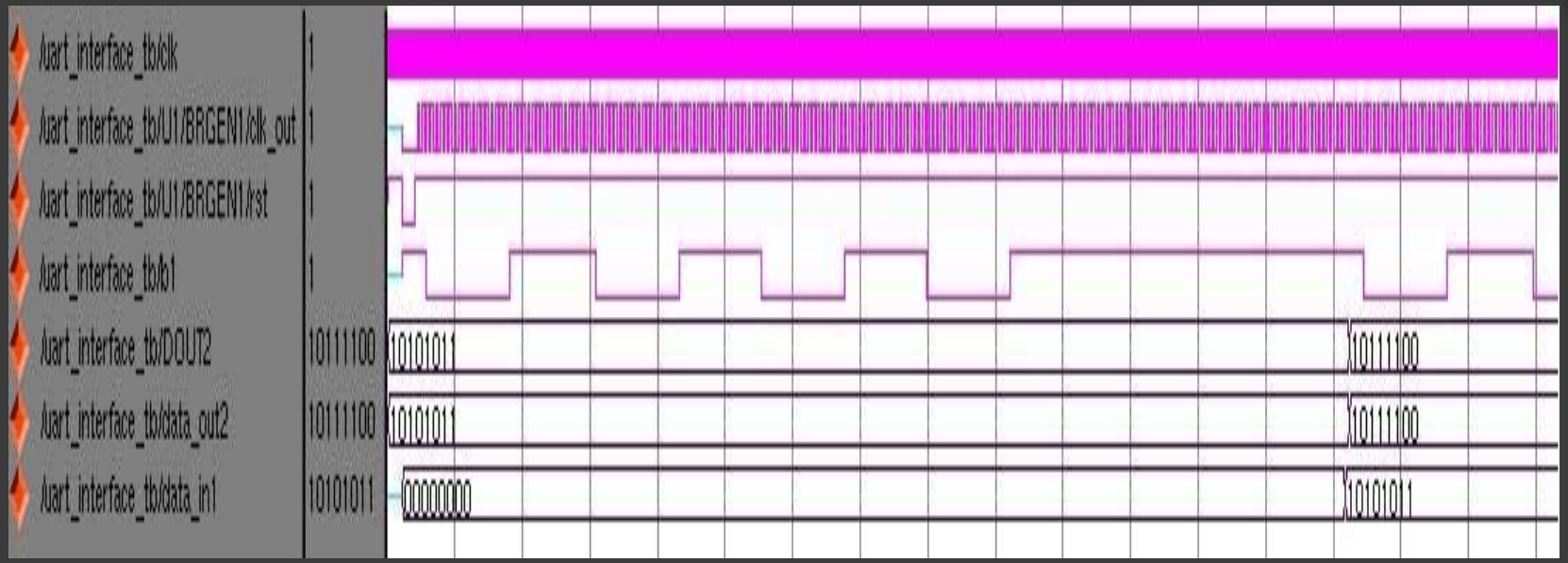
Incoming data is always stored in first cell of FIFO. After data is stored, shifting of data is performed. Because of this shifting, first inputted data would be always first to out.

Baud rate generator activation



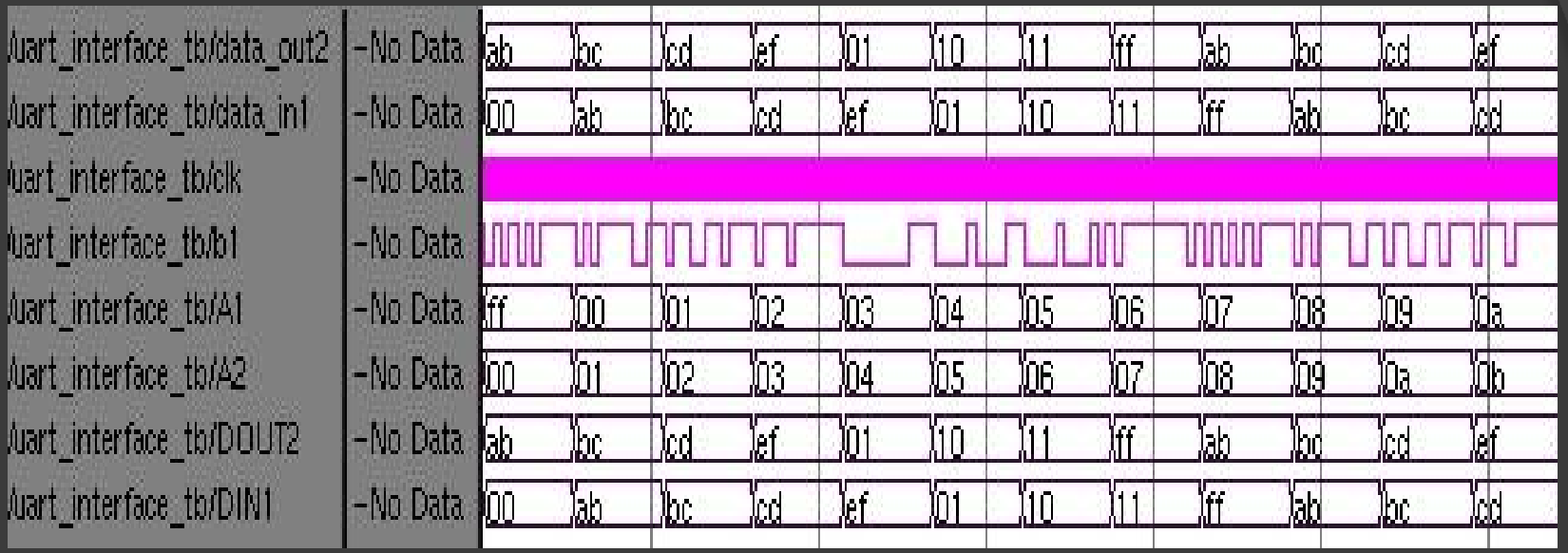
To make baud rate generator operate we need to activate it. This picture shows activation process. Low level on RST input starts UART. After activation low level on RST resets UART.

Transmitting 1 byte



This figure shows transmitting 1 byte (10101011) with UART

Data exchange

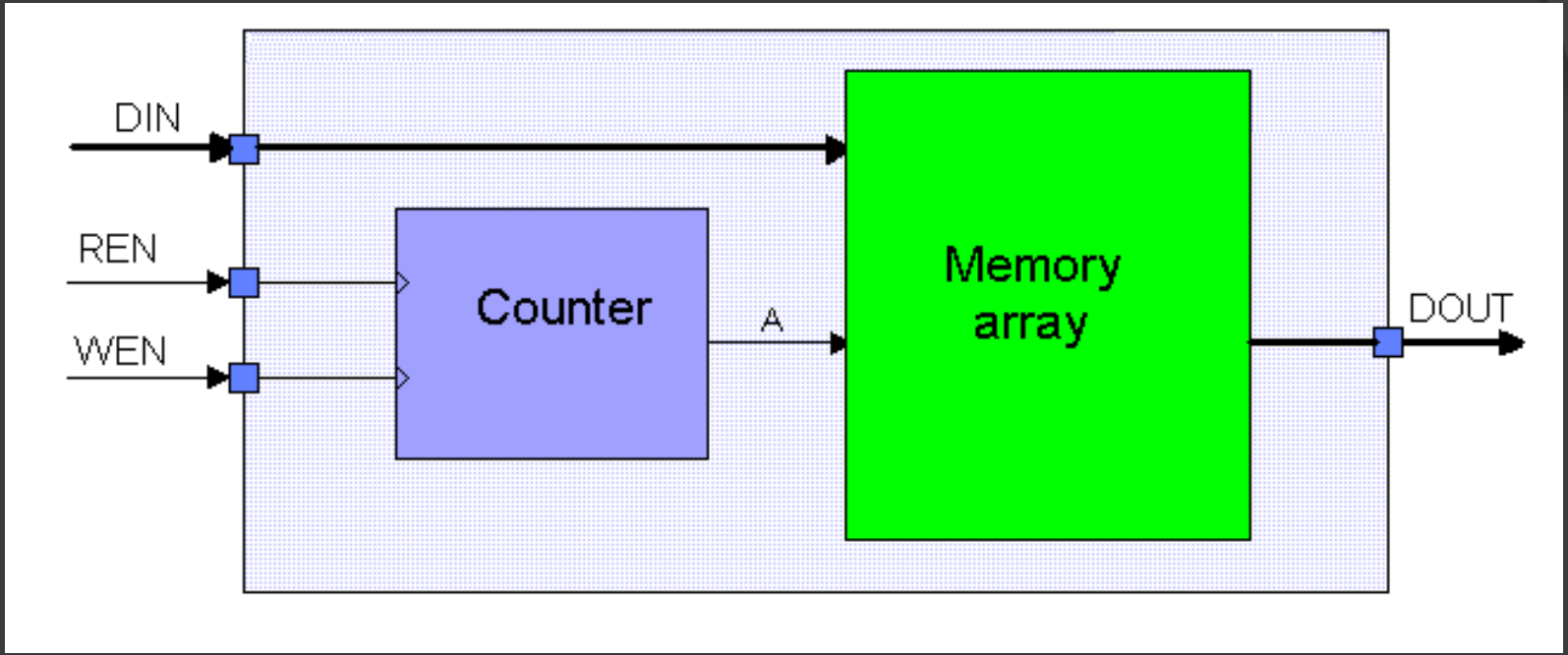


In this time 2 UART was connected to each other. First UART was transmitting data from 8x256 memory, and second UART was receiving incoming data and stored it in its empty memory.

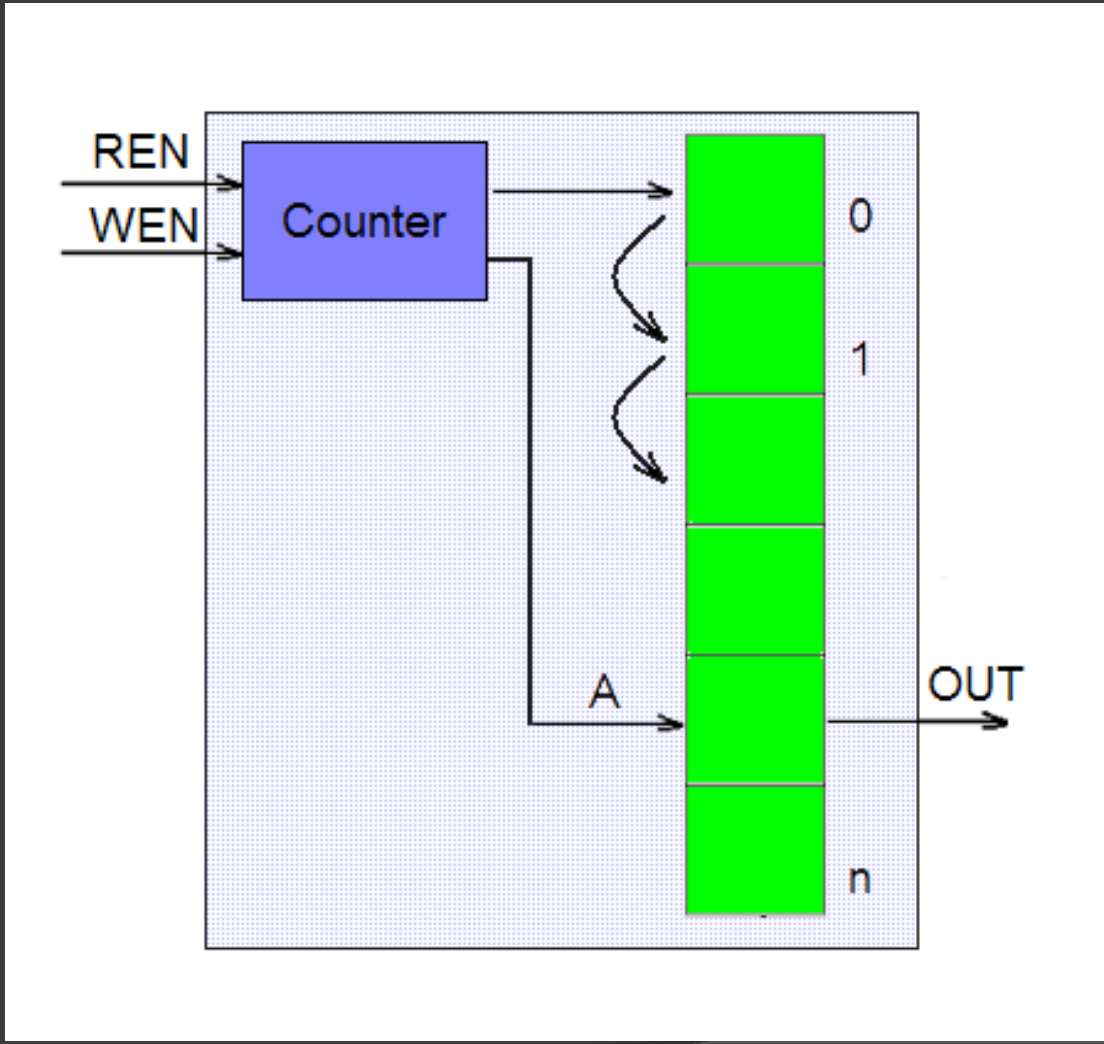
Synthesis

- Synopsys Design Compiler was used for UART synthesis.
- Two different UART projects are compared with area and power consumption.

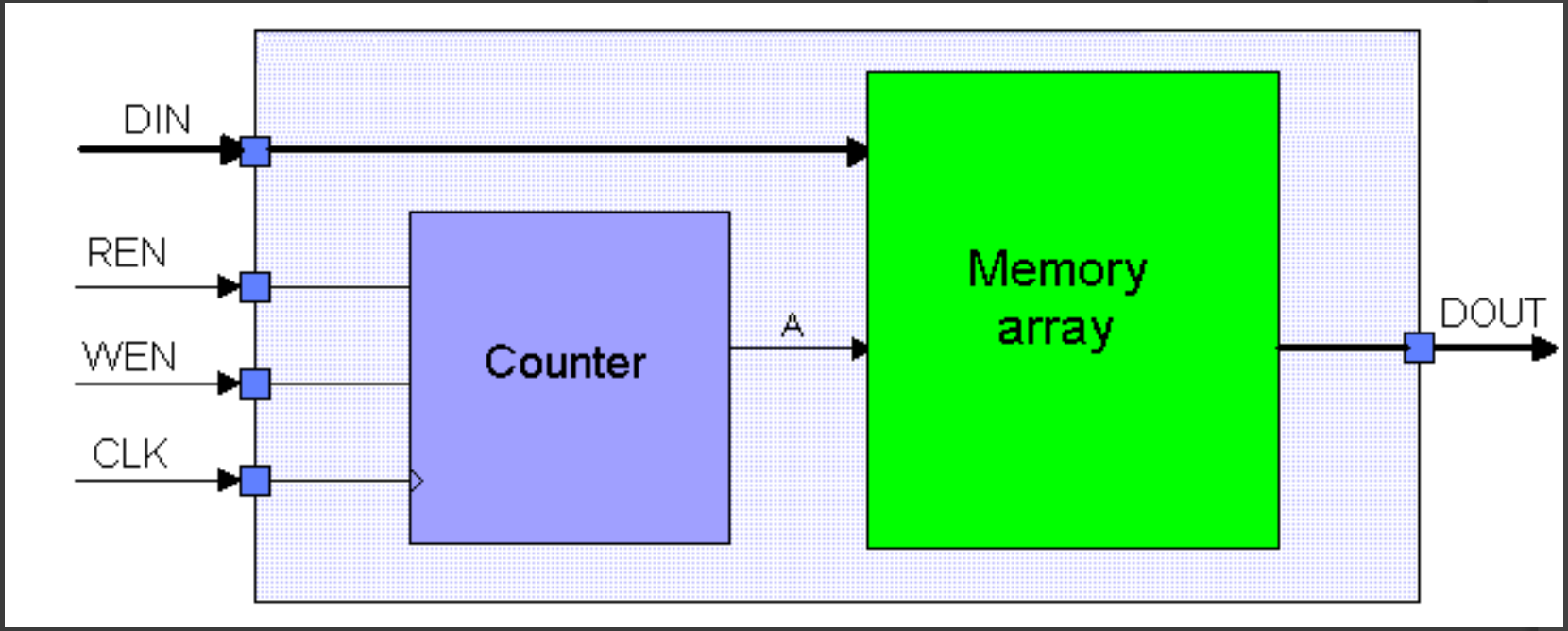
FIFO buffers structure



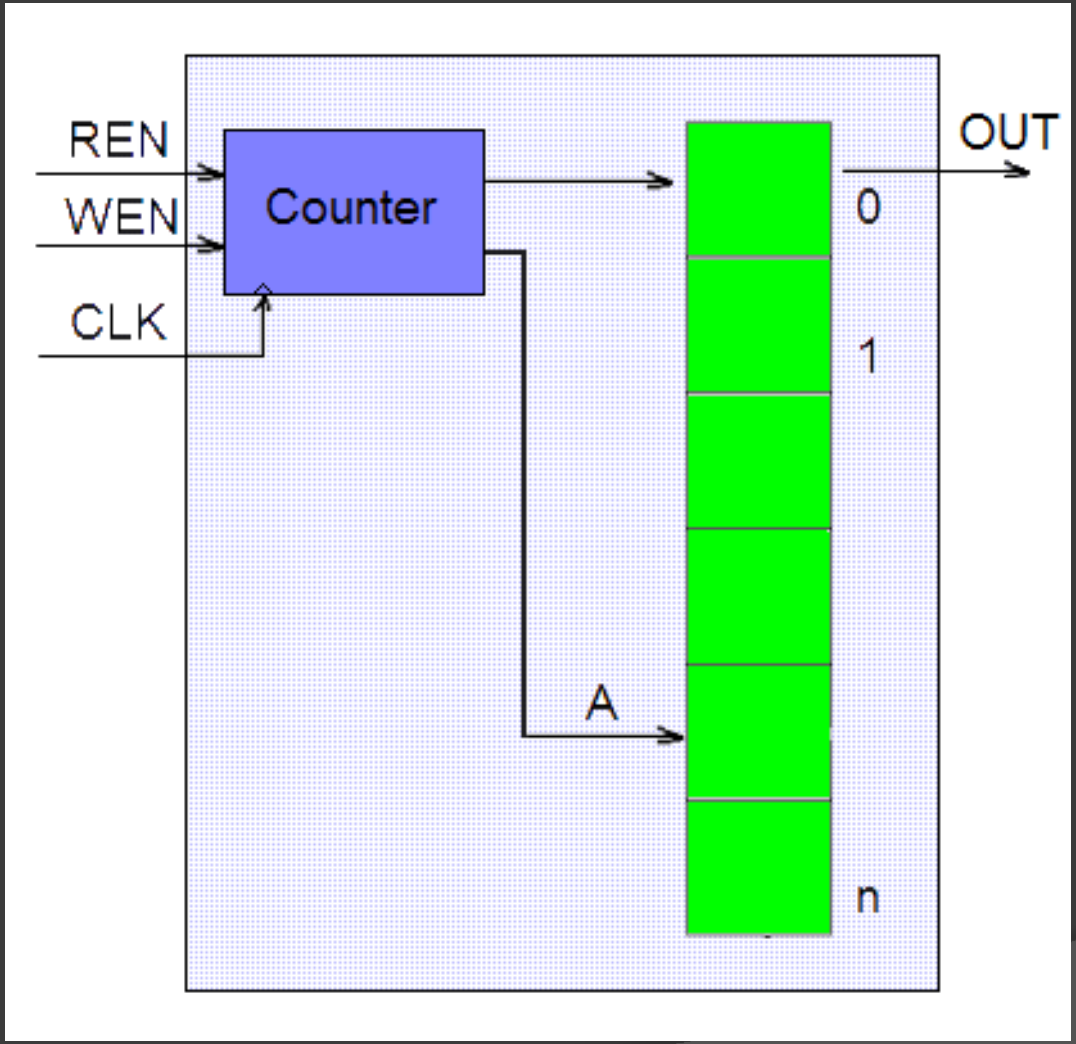
FIFO buffers structure



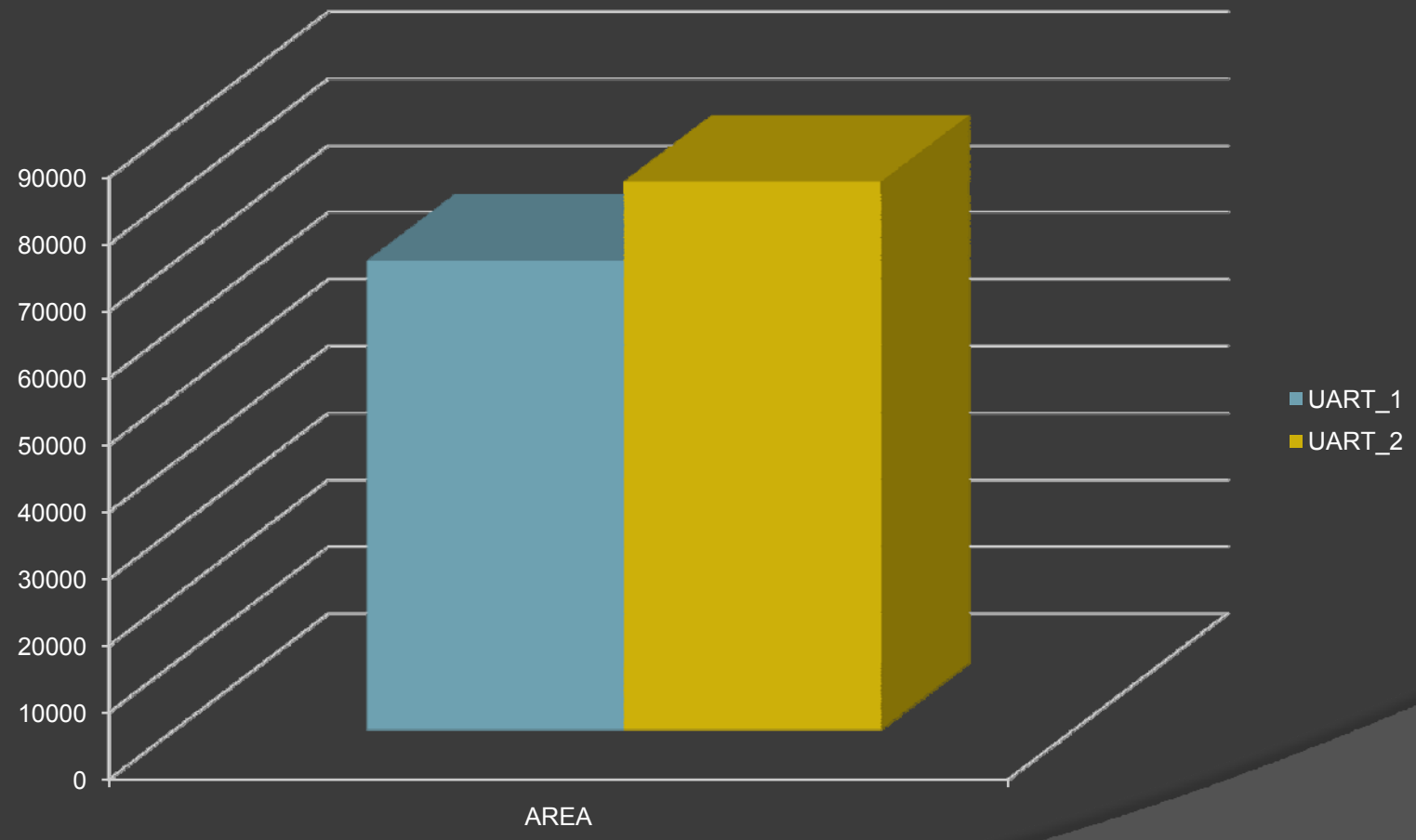
FIFO buffers structure



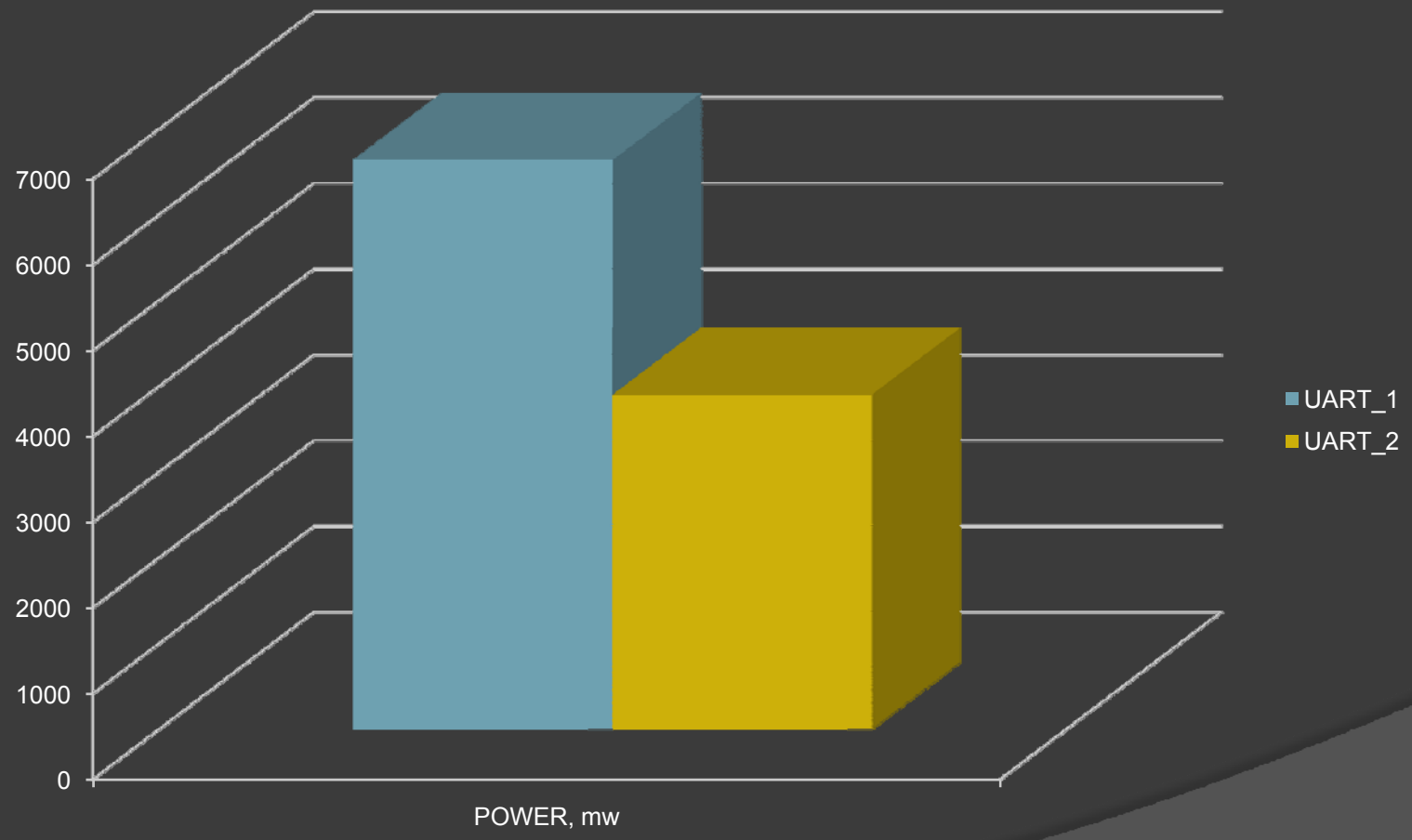
FIFO buffers structure



Area of device



Power consumption



THANK YOU FOR YOUR ATTENTION