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IC Synthesis and Optimization Challenges and Solutions

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Contents

Synthesis and Optimization Challenges and Solutions on the example of 90nm EDK

IC Design Challenges: Complexity

Routing congestion

Design complexity causes number of synthesis challenges and one of them is routing congestion. Routing congestion is a situation occurred during physical synthesis when the recourses for routing are not sufficient for routing required number of connections. For estimation of routing congestion in the design the following concept is used. Design is divided into relatively large grids where edges are anticipated for passing of dozens of wires, which defines routing resources. Then virtual routing is performed during which the number of wires which are required to pass through each edge is calculated. During this calculation wire crossings is not considered. Then on each edge overflow of resources and requirements is calculated as a difference between routing resources and routing requirements. Negative overflow means that there is routing congestion.

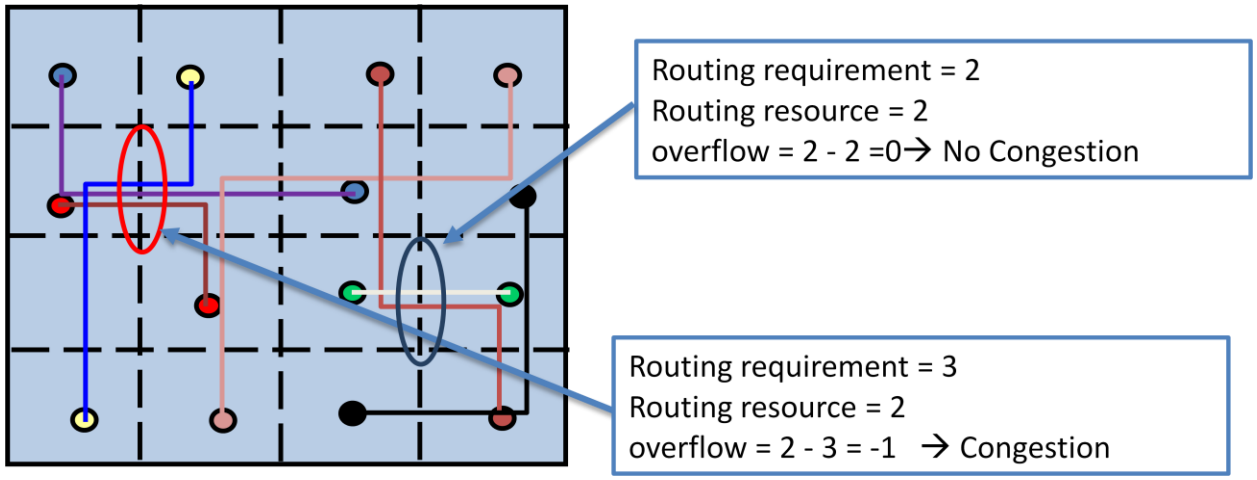

Figure 1 Routing congestion

For example, if routing requirements for some edge equals 2, routing resource is also 2, then overflow is 0, meaning that it is possible to route these wires, in another example overflow is negative as the number of required routing wires exceeds resources.

The issue of reducing excessive congestion in local regions such that the router can finish the routing successfully is an important problem. When solving the placement problem, traditional algorithms mainly focus on minimizing total estimated wire-length to obtain better routability and smaller layout area. However, a placement step is required to be congestion-aware and user should have possibility to address congestion issues early in the design, before starting actual routing, as congestion is more affected by placement.

Modern physical synthesis tools perform some congestion optimization that has a reasonable chance of providing acceptable congestion. Congestion increases efforts of placement algorithm. On average,

congestion awareness increases runtime by 20%. For user input modern physical synthesis tools, as a rule, have congestion map. The congestion map depicts congestion figure. The map shows scaling of congestion indicated to numerical values of congestion and corresponding colored gammas. It allows the designer to improve congestion in a dialog mode. The designer indicates the area of high congestion (on the map and the tool places the cells aimed at reducing congestion applying iteration algorithms.

Sources of Congestion and Solutions

Congestion can occur in standard cell placement regions and around IPs. High placement density can cause congestion, as in this case number of cells, subsequently number of pins that must be routed is large and obviously, there can be lack of routing resources. This problem is solved at physical synthesis stage with minimizing placement density.

Its negative impact on congestion can also have bad standard cell and IP pin access, because bad pin access means that the physical synthesis tool is forced to use much more resources for touring the given pin. Of course, the solution must is considered during Standard Cell Library development.

Bad pin access impact is determined by the following peculiarities of the routing process. It is common to draw consequent metal layers perpendicularly, because it enables the tool to draw wires of the same layers parallel. The advantages are: large number of wires and possibility to route on the tracks, which simplifies routing process and saves run time. From this perspective congestion means that number of tracks is not enough for routing. So bad pin access for cells can require more tracks to be used.

In case of standard cells the problem occurs when more than 2 pins are located on the same track, the

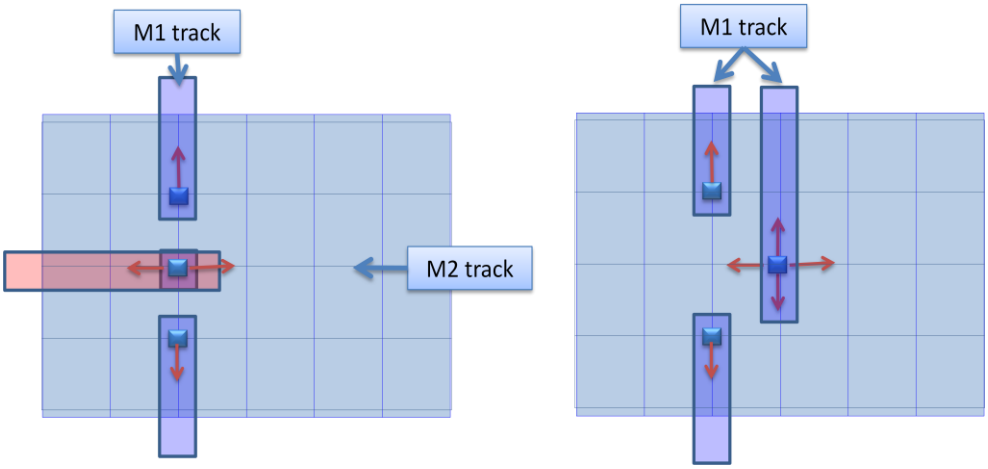

Figure 2 Standard cell routability improvement

tool will be forced to route the third pin with upper layer net. To avoid this, the cell must be designed so, that the number of pins on the same track doesn't exceed 2. In this case the routing of the third pin can be done with the same layer, thus leading to better utilization of the lower layer tracks.

Typically IPs have large number of pins that are placed close to each other, subsequently large number of wires will be needed for routing them. If the pins are on the same layer one track will be needed for each pin connection. This will lead to problem, when large number of local tracks is used causing congestion for the cells in the region.

A possible solution is to create the same pin of the IP on several layers. In this case tool will not be forced to use a certain layer and will be able to choose a track that is less likely to cause congestion.

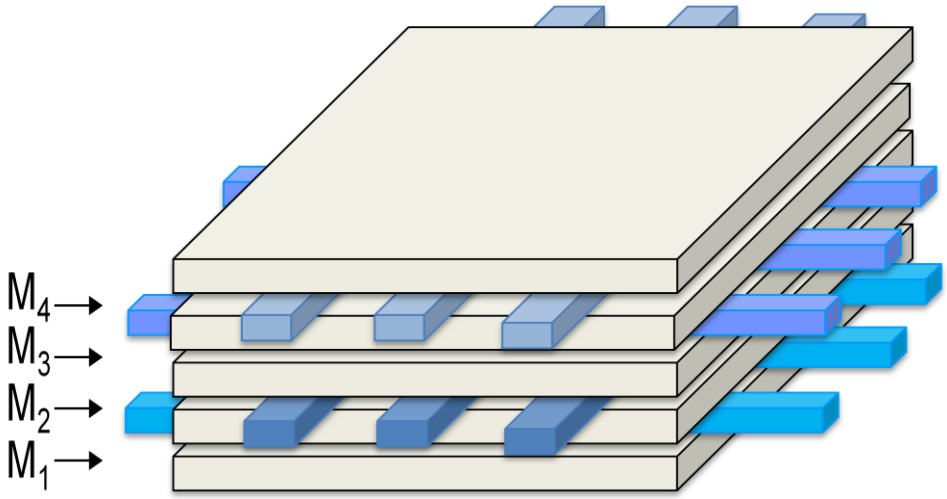

Figure 3 Pin availability on several metals

Advanced I/O Cell Placement

Another important challenge today is related to advanced I/O cell placement. This depends on IC pin packaging method. Currently two methods are used, first and the classic one is wire bond connection, another is flip-chip.

Wire Bond

Wirebond is the most widespread method and is characterized by connection of package pins to IC pins by wires. This is classic method and requires from IC designer to place special connection pads around the IC where wire connection can be made.

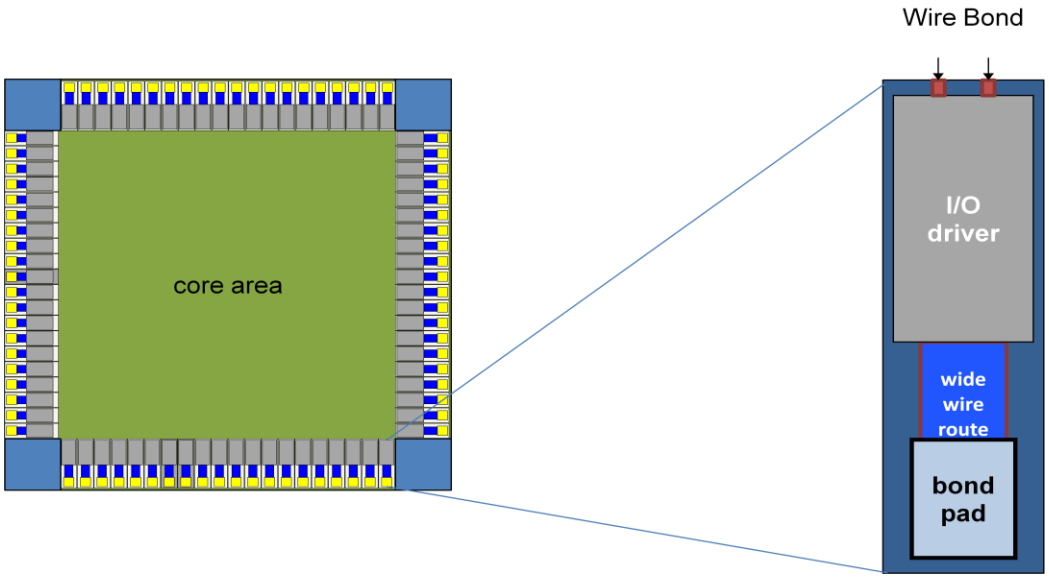

Figure 4 Wire bond placement

For classic wire bond connection I/O cell structure is shown. The I/O cell is composed of I/O driver, which is the actual cell performing required I/O functions and bond pad which is used for wire bond connection. These cells are placed around the edges of IC.

The modern version of package-to-IC connection is called flip-chip. In this method IC is connected to package by use of solder balls which are placed between package pins and IC pads. In this type of assembly IC itself is placed flipped, that is the name flip-chip. This poses additional challenges on I/O designer and IC design tools.

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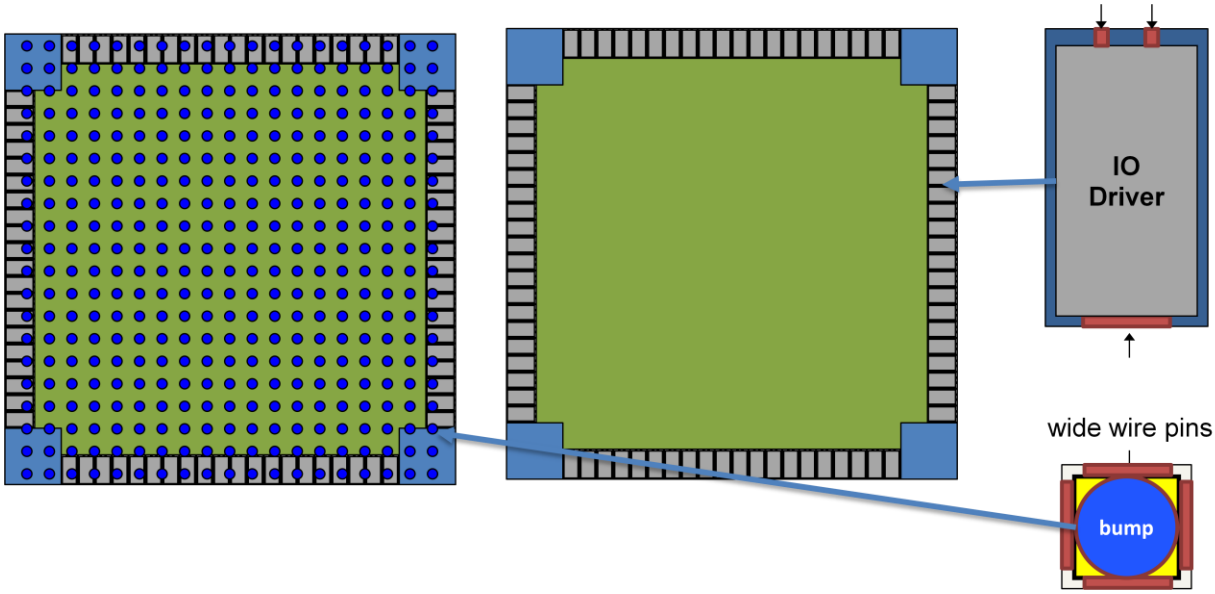

Figure 5 Flip-chip connection

For flip-chip design connection is made not only around the edges but also on top of whole IC. In this case pads are called bumps. But the actual circuitry, the I/O drivers are placed near edges. Thus this method requires from I/O developer to create separate drivers and bump cells.

IC Design Challenges: Design for Manufacturability (DFM)

Metal Density

Design for manufacturing (DFM) is a development practice emphasizing manufacturing issues throughout the product development process. DFM includes a set of techniques to modify the design of ICs in order to make them more manufacturable, i.e., to improve their functional yield, parametric yield, or their reliability.

Technological processes used in current technologies like etching require that underlying dies will be as much uniform as possible for reproduction of good results.

As wires are obtained in subtractive process, when at first a sheet of metal is laying down and then removing what is not needed. Depending on density, this may take more time to etch. Total etch time is set by the low-density regions, because enough time is needed to finish clearing out the metal. If metal density is too low, etch time becomes severe. Due to long etching times some structures can suffer of over-etching. To avoid this, some dummy metals can be added at low density region. Fill cells can be used to increase metal density in which wires are tied to Vdd or Gnd. So the necessity for checking density is the following: Density affects etch rates as described in the previous slides. Also large variations in density can cause thermal expansion stress. To solve these problems density rules must be used.

Dummy Metal Fill Utility

To meet minimum density rule dummy metal fill is implemented. This is done by a special utility which fills low density spaces with dummy metal tile pattern achieving average density which is somewhere in between maximum and minimum allowed values. Density of metal usage has a minimum and a maximum constraint. Limits are typically 30% < density < 80% for metal. Density needs to be checked both globally and locally.

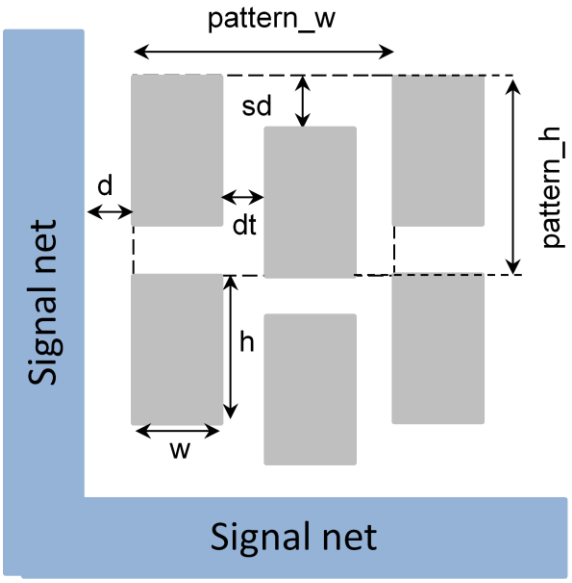

Figure 6 Dummy metal fill example

In SAED 90nm EDK density fill utility was created based on Synopsys IC Validator tool. The utility checks for density violations in the design and fills low density regions with dummy metal tiles. Its only function of which is to bring the design to a uniform density. This utility brings design metal density to around 53%. This is average between 30 and 80 percent limits of density rules.

Metal Fill Estimation

Another issue related to density issue is that parasitic extraction of layout databases containing metal fill objects can make runtime and memory requirements unacceptable. To solve this problem an approximation can be made for the capacitive effects that proximal floating metal objects can have on routed signals in the design simply and effectively in the interconnect technology file (ITF) file. StarRC ITF metal fill modeling is designed to estimate the capacitive effect of small, floating fill shapes within the routed core area. This effect is calculated by embedding dummy tiles in the empty areas of the core (according to the fill specifications).

Metal fill estimation that is implemented in STARRC enables to estimate two types of parasitic capacitances possibly caused by dummy metal fill tiles. When the dummy is placed between two metal layers and when it is inserted amongst two parallel layers. As I already mentioned, we have created metal fill utility , and ITF file was also created that represents parasitic effects of such metal filling and evaluation shows that the difference between estimated and real results is about 13%.

Antenna Effect

IC manufacturers required antenna rules to ensure that the transistors of the chip are not destroyed during fabrication. When a metal line is fabricated, it can act as an antenna. Reactive ion etching causes charge to accumulate on the wire. If the amount of these charges on the wire is too large, and if it is connected only to the gates of transistors (not to source or drain or any other active material), the charges will be enough to blow the oxide under the gate of transistor. If the ratio of the poly or metal layers to the area of the transistors is too large, the transistors will be destroyed.

One fix is to add bridges to the layout. The long wire “must see” diffusion first, and gate second. Wires are built from the lower layers up and cost the routing resources on the upper metal layers. This is not a very common way to fix antenna violations.

A piece of “drainage” diffusion can be added near the gate to avoid this problem. This reversed-bias diode does not affect chip operation; because the substrate is tied to ground no current will leak through this diode. During fabrication, it allows charge to drain away harmlessly. Area of diode is set by ratio of wire perimeter and gate area. This is the common way to fix antenna violations.

Antenna rules work incrementally and should be checked incrementally. First only M1 rules are checked, and then M2 is added and checked, etc. Most favorite DRC tools allow calculating incremental antenna rules.

Contemporary automated physical synthesis tools, such as Synopsys IC Compiler, are able to automatically fix antenna violations. To perform antenna fixing, the tools need additional information to be given as an input. Engineers provide the tools with Antenna rules and Antenna properties in CLF format for each standard cell, I/O cell and IPs. The tool calculates violation based on the rules and automatically inserts Antenna diodes where needed. The Antenna diode cell must be present in the Digital Standard Cell Library used for the design.

Electromigration effects

Nowadays, issues caused by electromigartion are very important. Electomigration effect, which is the effect when current density exceeds the threshold value, the transport of atoms occurs in a metallic interconnect along the direction of electron flow.

Electromigration can cause two types of failures: Void (open circuit failure), when in narrow interconnects, like those linking transistors and other components in integrated circuits a break or gap can develop in the conducting material, preventing the flow of electricity and Hillock (short circuit failure), when atoms of a conductor pile up and drift toward other nearby conductors, creating an unintended electrical connection. The role of electromigration phenomenon which has always been present in ICs, for 90nm technologies and below considerably increases and is one of the main challenges. A reduction of the structure (scaling) by a factor k increases the power density (and thus the temperature) proportional to k and the current density increases by k2 whereby EM is clearly strengthened. In order to prevent electromigration, technologies often restrict IC designers by providing limits for current densities in wires and their dependence on temperature.

In current physical synthesis tools it is possible to run signal net electromigration analysis and correction.

The complete EM analysis an fixing flow is divided into two stages. The objective is to minimize data handling. In the first stage, switching activity analysis is performed. Based on its results, nets that are not prone to EM are filtered out. In the second stage, detailed EM analysis on the remaining nets is performed. At this stage another input called EM Rule File is needed that has information of EM threshold current density at average, peak and etc. Finally EM rule violations are automatically fixed.

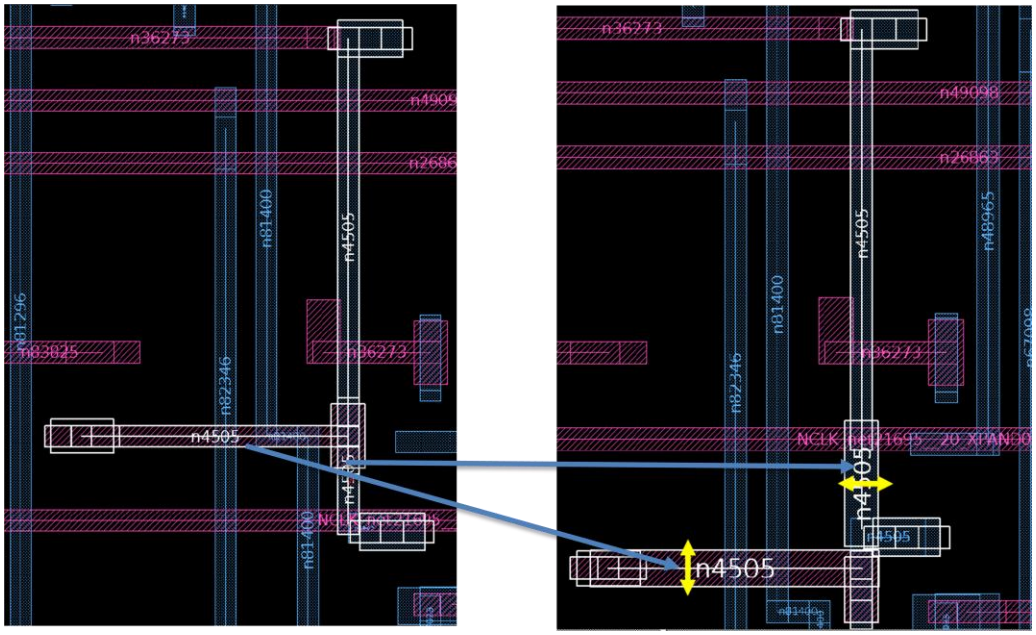

Figure 7 Electromigration fixing example

An example of EM fixing, which was done using the EM rule created for SAED90nm EDK is shown. During the EM analysis the tool has detected that the width of net n4505 (on the figure at the left) is not enough for its current density and it is prone to EM failure. Thus the width of the net was changed.

SAED 90nm Educational Design Kit (EDK)

Solutions for above mentioned challenges were implemented in 90 Educational Design Kit (EDK). It contains Digital Standard Cell Library, containing 340 cells, including all necessary special cells and other changes described, also whole library is available in 3 versions with standard, low and high threshold voltages. Also EDK contains Input/Output cell consisting of 50 standard cells and 3 special cells designed according to contemporary standards like PCI, etc.

EDK contains Phase Locked Loop cell which is also one of the essential components for IC design. EDK also contains set of Static memories of different sizes. All these components allow designing ICs of different complexity. Moreover, the EDK contains reference designs of different processors as examples.

Technology Kit

In 90nm Technology Kit all the documentation needed for design is created including design rules, GDSII, Layer Map, Device Formation rules and Process Description. Spice models and Milkyway technology files are also present. In addition, all files needed during the design flow, such as CosmosSE generic symbols library, pcells, Hercules DRC and LVS decks and StarRC parasitic extraction files are provided.
Moreover, number of scripts is written which support design flow.

Digital Standard Cell Library

The Digital Standard Cell Library developed at SAED has been built using 90nm EDK 1P9M 1.2V/2.5V design rules. The library has been created aimed at optimizing the main characteristics of designed ICs by its help. The library includes typical miscellaneous combinational and sequential logic cells for different drive strengths. Besides, the library contains all the cells which are required for different styles of low power (multi-voltage, multi threshold) designs. Those includes: Level Shifters, Isolation Cells, Retention Flip-Flops and others. The presence of all these cells provides the support of IC design with different core voltages to minimize dynamic and leakage power. Cell list compiled on the basis of analysis of different educational designs, contains all cells needed for educational purposes. Digital Standard Cell library contains 340 cells.

Characterization Corners

Besides special cells for low power libraries, additional characterization corners should be added (lower part of the table) in addition to the standard characterization corners used for regular libraries. These are needed because special cells need to be placed in non-regular operation modes, like low voltage blocks and need to be characterized for these modes. SAED90nm DSCL was characterized for the 16 process/voltage/temperature conditions shown in table. Composite Current Source (CCS) modeling technology was used for cell characterization to meet the requirements of contemporary low power design methods. CCS provides timing, noise, and power analyses while considering the relevant nanometer dependencies. Also some additional corners were used to characterize level shifters - both low-to-high and high-to-low. There are 12 corners for each type.

I/O Cell Library

The I/O Standard Cell Library supports the design of different integrated circuits (ICs) in 90nm technology. The cells in the library include a complete set of standard functions. It contains 36 cells , and all are 65um x 300um in size or smaller.

Phase Locked Loop

SAED_EDK90_PLL aligns the rising edge of the reference input clock to a feedback clock using the phase-frequency detector (PFD). The falling edges are determined by the duty-cycle specifications. The PFD produce

an up (UP) or down (DN) signals that determine whether the voltage controlled oscillator (VCO) need to increase or decrease its frequency.

The PFD output applied to the Charge pump (CP), and consecutively to Low pass filter (LPF), which produces a control voltage for setting the VCO frequency. If the PFD produces an UP signal, then the VCO frequency should increase. A DN signal decreases the VCO frequency. If the CP receives an UP signal, current is driven into the LPF. Conversely, if it receives a DN signal, current is drawn from the LPF.

The LPF also removes glitches from the CP and prevents voltage over-shoot, which filters the jitter on the VCO.

Feedback divide counter is inserted in the feedback loop to have the VCO frequency multiplied by divide factor. VCO frequency (fVCO_OUT) is equal to 4 times of the reference signal frequency (fREF_CLK).

The VCO output feeds up to two post-scale counters (Output dividers). These post-scale counters allow a number of harmonically related frequencies to be produced within the PLL.

Conclusion

Today, while designing advanced ICs, engineers face lots of challenges. For number of challenges possible solutions were implemented in SAED 90nm EDK. SAED 90nm EDK has number of peculiarities such as ability to support low power designs, however, the first and most important one is that the EDK was created for educational purposes in universities worldwide and Synopsys customer training, that is why it is free from Intellectual Property restrictions. The EDK made it possible for SNPS university program members to use Synopsys tools that they receive within the cooperation framework and develop modern advanced designs.

Although the designs with 90nm EDK are not for fabrication, the results are close to real ones. The number of designs done at different universities testifies to that the EDK can really handle complex ICs (such as OpenSPARC and ChipTop processors) while addressing number of design challenges.