Methods for Analysis of Robustness and Reliability of ICs

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Institute for Electronic Design Automation

TU München

Agenda

- **Institute for Electronic Design Automation at TUM**
- Reliability Analysis (D.Lorenz)
    - Aging Effects on Digital Circuits
    - Aging Analysis on Gate and Register-Transfer Level
    - Aging Monitors
- Robustness Validation (Martin Barke, Martin Radetzki)
    - Measuring robustness
    - Robustness as a probability
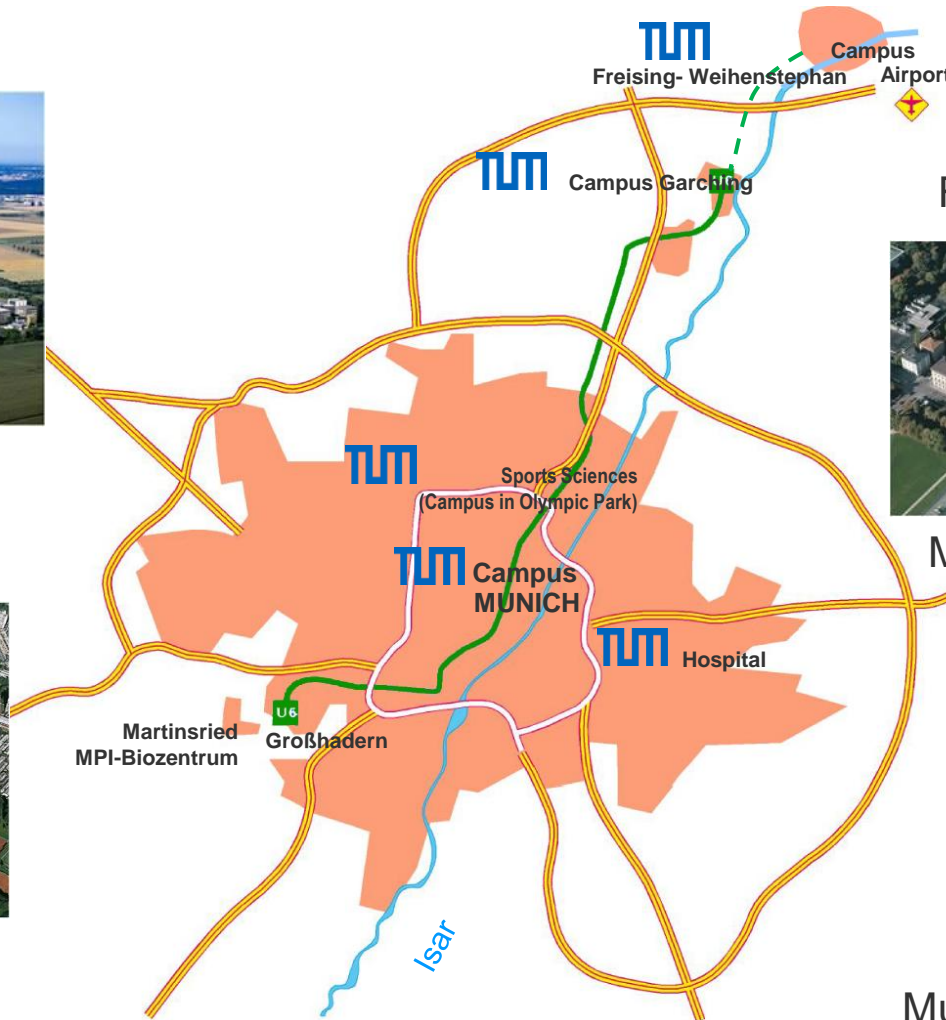   - Robustness of Digital Circuits

München / Munich

TU München

Freising- Weihenstephan

Campus Airport

Campus Garching

Freising-Weihenstephan

Garching

Sports Sciences
(Campus in Olympic Park)

Munich, Downtown

Campus MUNICH

Hospital

Martinsried
MPI-Biozentrum

Großhadern

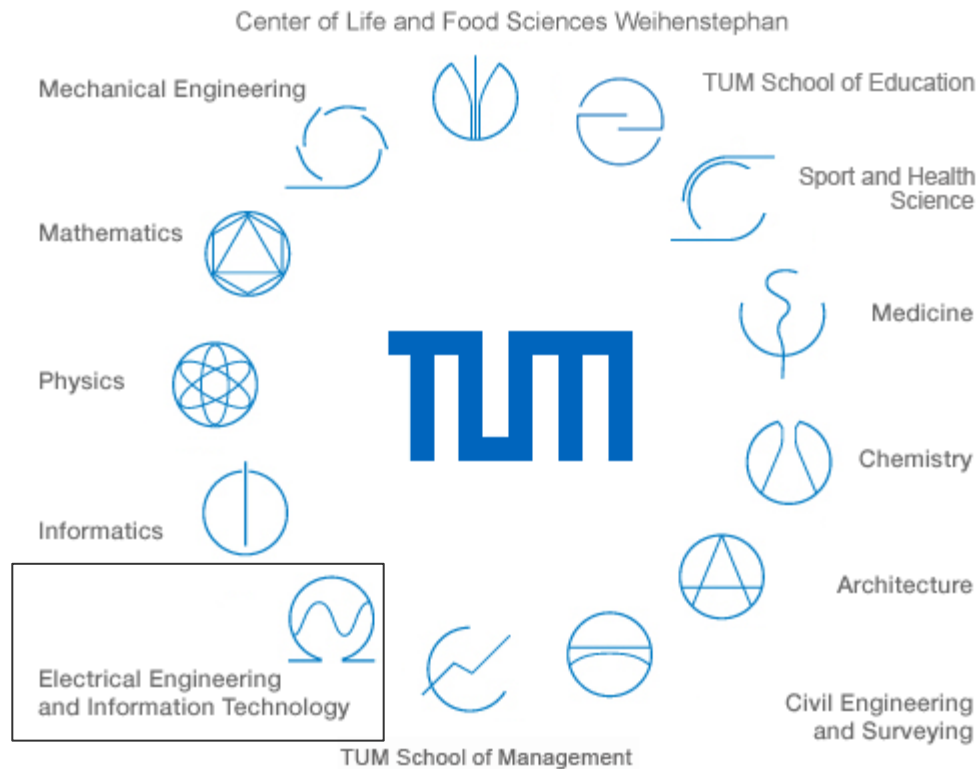U6

Isar

Munich, Olympic Park

Munich, TUM Hospital

TU München

- Total Students ~25000
- Students starting each year ~6500
- Students graduating each year ~3500
- Professors ~400
- Researchers ~5000
- Non-scientific staff ~2900

TU München - Departments

Center of Life and Food Sciences Weihenstephan

Mechanical Engineering

TUM School of Education

Sport and Health Science

Mathematics

Medicine

Physics

Chemistry

Informatics

Architecture

Electrical Engineering and Information Technology

Civil Engineering and Surveying

TUM School of Management

Electrical Engineering and Information Technology

- 2250 Students
- 37 Professors
- 329 Researchers (56% paid from 3rd party funding)
- 134 Non-scientific staff
- German study programs
  - B. Sc. in Electrical Engineering and Information Technology
  - M.Sc. in Electrical Engineering and Information Technology
- English study programs
  - M.Sc. in Communications Engineering (MSCE)
  - M.Sc. in Power Engineering (MSPE)
- Research fields
  - Electrical Power Engineering
  - Information and Communication Technology
  - Microelectronics
  - Circuits and Systems
  - Automation and Autonomous Systems

Institute for Electronic Design Automation

- 1975 first German university EDA institute
- 21 members (15 PhD candidates)
- EDA tools and design methodology
- 2002: spin-Off MunEDA (www.muneda.com) (WiCkeD)
- 3rd party funding: Funding: BMBF, DFG, industry
- Industry partners: Infineon, Intel Mobile , Bosch, Atmel, Freescale,
- University partners: Berkeley, Bogazici Istanbul, Carnegie Mellon, KU Leuven, Sevilla
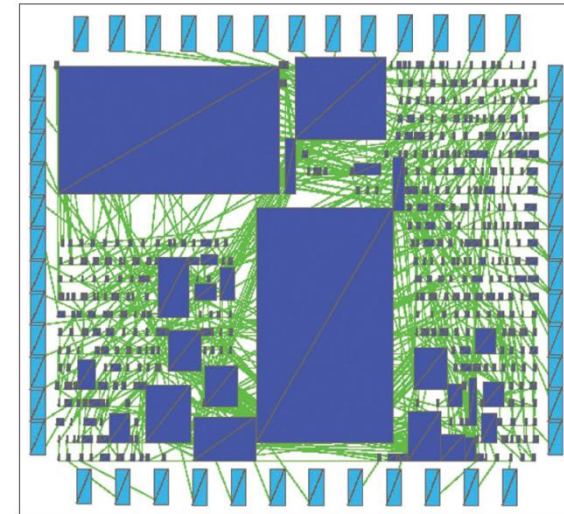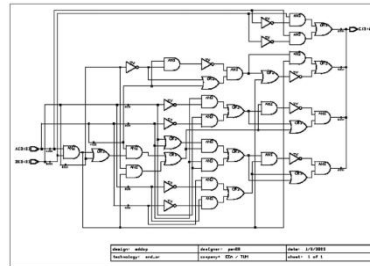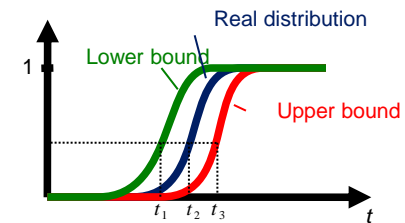
Institute for EDA
Prof. U. Schlichtmann, PD H. Graeb
http://eda.ei.tum.de
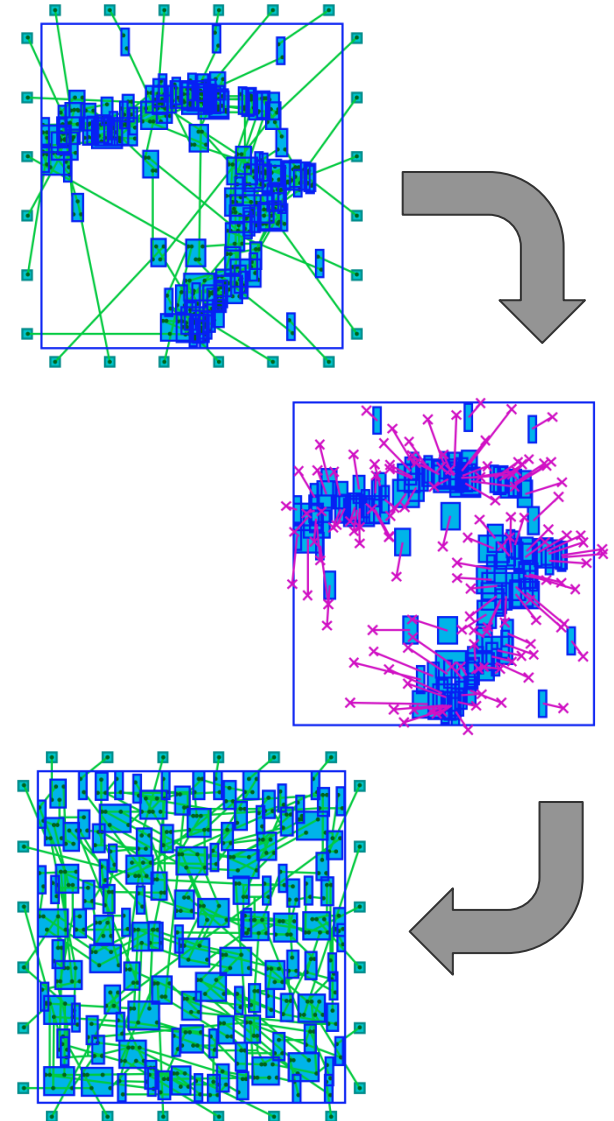
Research Areas

- Physical design
- Statistical timing analysis
- Reliability analysis
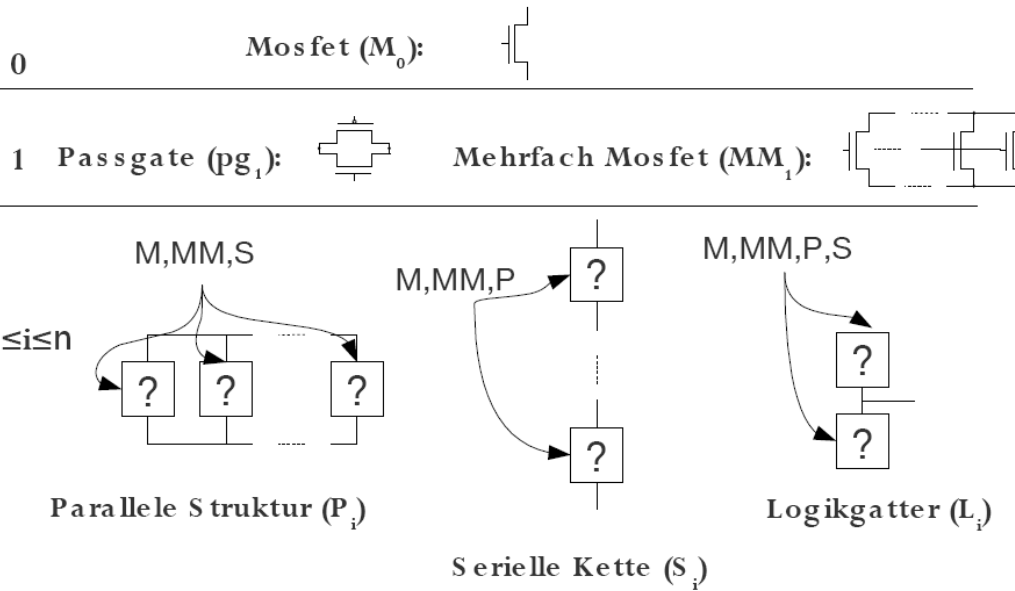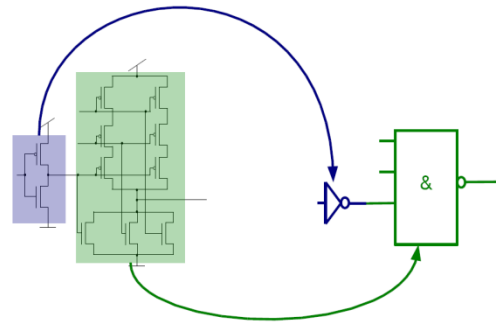- High-level modeling/Virtual prototyping
- Analog EDA
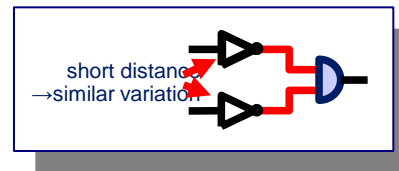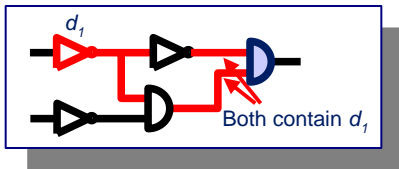
Layout Synthesis

- Fast placement of a circuit on a chip with minimal total netlength and no cell overlap

- Kraftwerk:
  - Circuit is spring system: Cells are attracted by free spaces and pushed by each other
  - Minimize quadratic netlength
  - Won Placement Contest of ISPD 2006

- Future task: placement of 3D-ICs
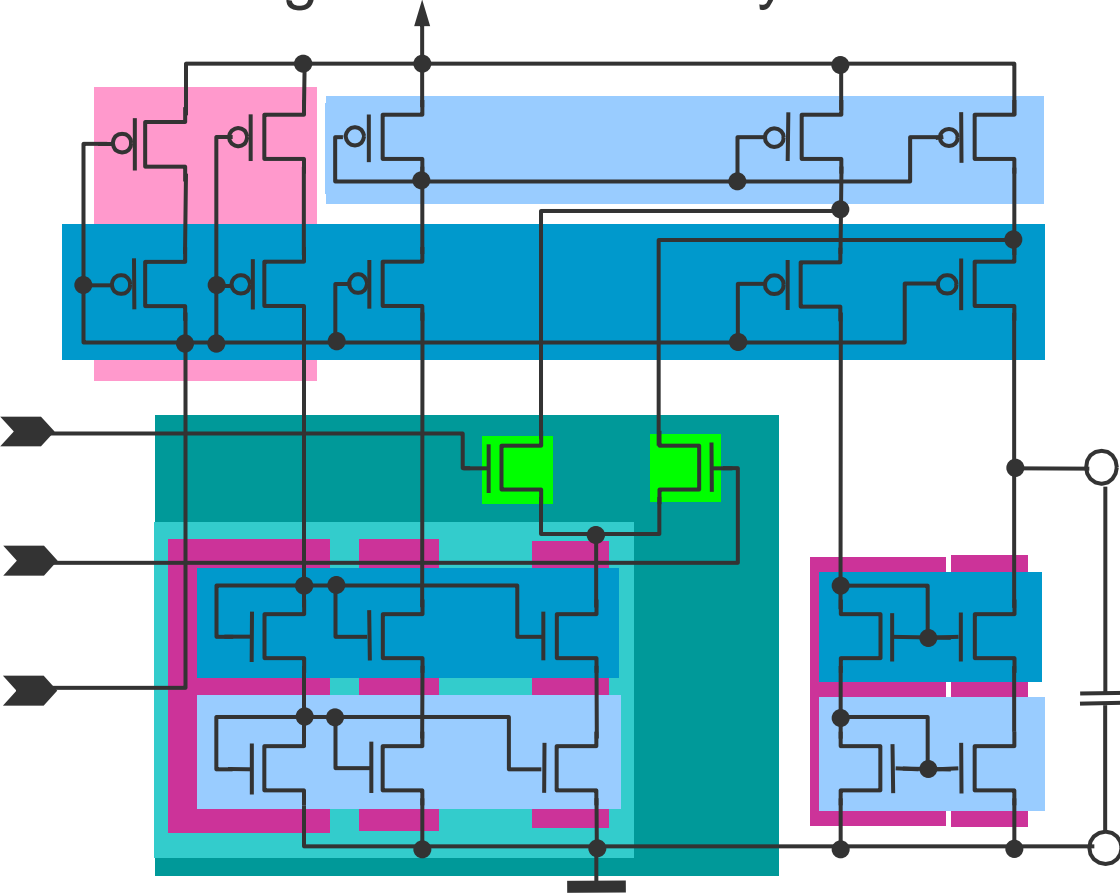
P. Spindler, U. Schlichtmann, F. M. Johannes, „Kraftwerk2 - A Fast Forced-Directed Quadratic Placement Approach Using an Accurate Net Model", IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 27, no. 8, pp. 1398-1411, August 2008

Structural Analysis of Digital Circuits


Mosfet (M_0):

0

1 **Passgate (pg_1):**   **Mehrfach Mosfet (MM_1):**

M,MM,S

$1 \leq i \leq n$

M,MM,P

M,MM,P,S

? ? ?

?

?

?

?

Parallele Struktur (P_i)

Serielle Kette (S_i)

Logikgatter (L_i)

Analog Structural Analysis

voltage reference 1

current mirror load

2-trans. current mirror

level shifter

differential pair

4-transistor current mirror

current mirror (bank)

level shifter (bank)

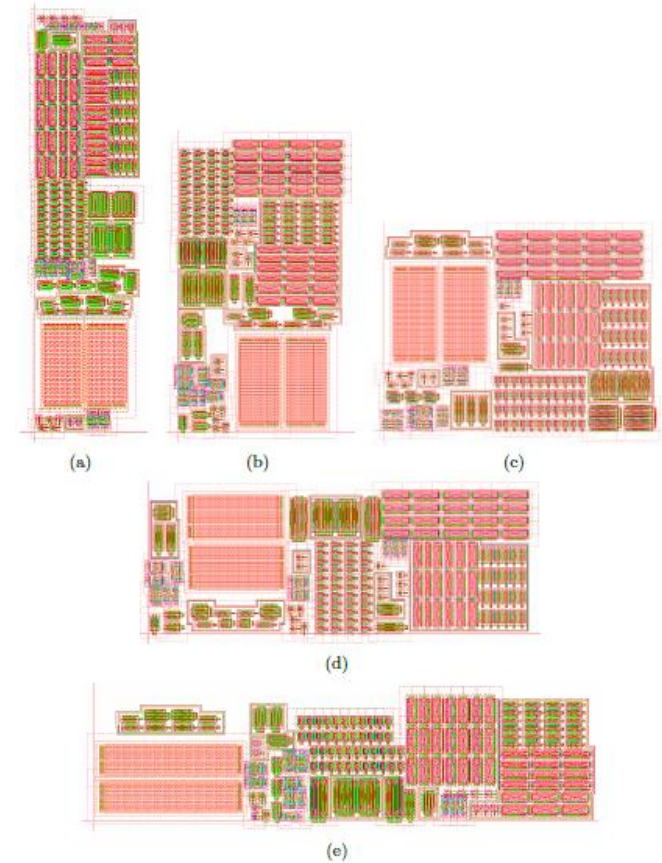cascode current mirror

casc. curr. mirror bank

differential stage

Analog Yield Optimization
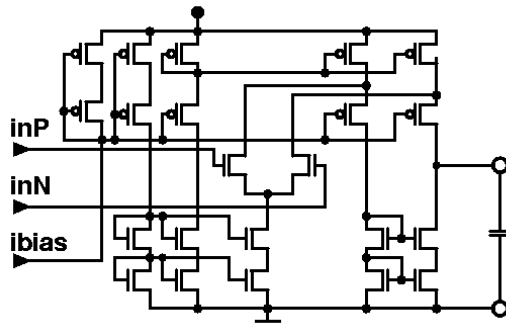
CPU time: 25min
(equal to 1 Monte-Carlo analysis)

| performance specification		initial		optimized	
gain [dB]	≥65	76	2.5σ	76	4.2σ
transit frequency [MHz]	≥30	67	7.7σ	58	4.5σ
phase margin [º]	≥60	68	1.8σ	71	3.9σ
slew rate [V/μs]	≥32	67	6.3σ	58	3.9σ
DC power [mW]	≤3,5	2.6	1.1σ	2.3	4.2σ
overall yield		82.9%		99.99%	

Analog Placement – Plantage

Source: M. Strasser: Deterministische hierarchische Platzierung analoger integrierter Schaltungen, PhD Dissertation, TU Munich, 2011

Virtual Prototyping

- Virtual prototypes based on Transaction Level Models (TLM):
  - Models of complete embedded systems (SystemC/TLM)
  - Platforms for early software development and design space exploration
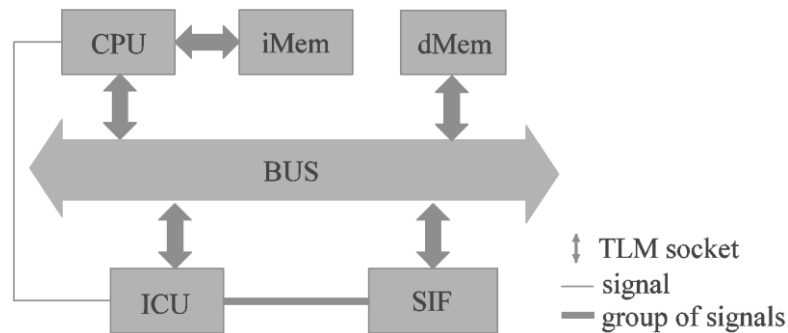
- Ongoing work: Non-functional performance estimation
  - Prediction of execution times of software on embedded processors.
  - Prediction of communication delays for large buffer transfers (TLM+ modelling style, BMBF SANITAS project)
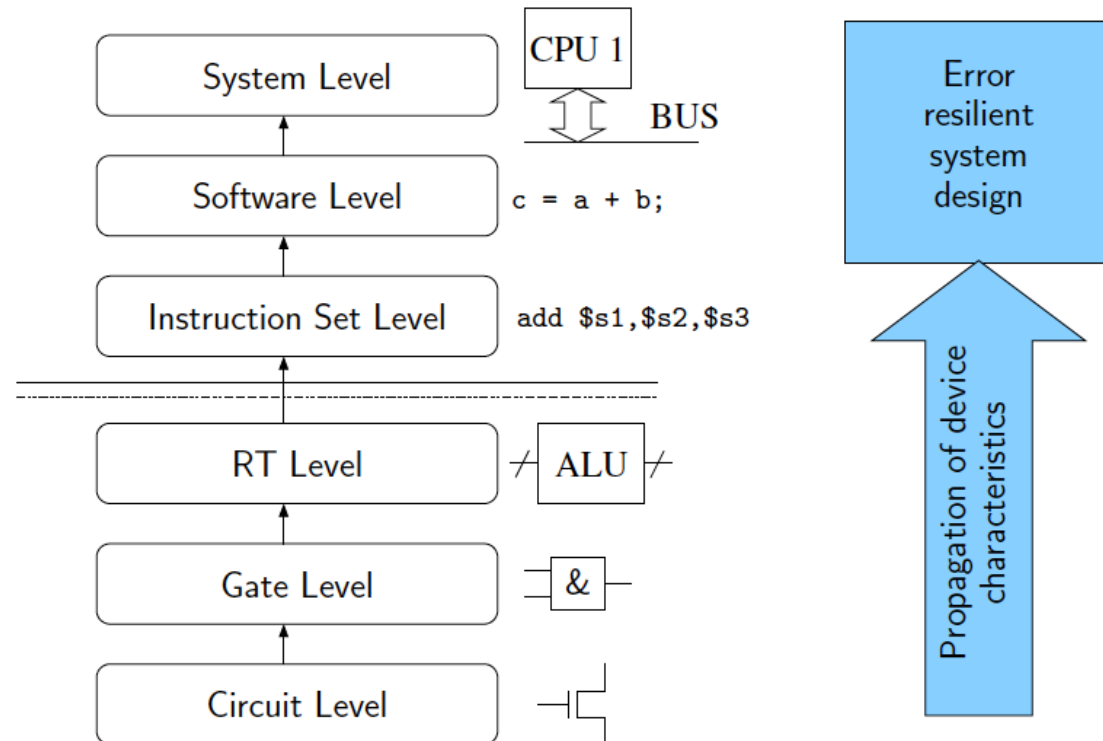 - Prediction of power consumption on task level.

Error-Resilient System Level Design

Problem:

• Process variation, radiation, etc. lead to an increasing uncertainty in device performances
• Traditional worst-case design becomes too pessimistic

Solution:
Accept errors at device level and handle them at higher abstraction levels

System Level	CPU 1
Software Level	c = a + b;
Instruction Set Level	add $s1,$s2,$s3
RT Level	ALU
Gate Level	&
Circuit Level	

Error resilient system design

Propagation of device characteristics

The goal shouldn't be to eliminate failure; it should be to build a system resilient enough to withstand it.
(Megan McArdle: In Defense of Failure. Time Magazin 11/2010)

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  - Measuring robustness
  - Robustness as a probability
  - Robustness of Digital Circuits

Reliable Systems from Unreliable Fabrics
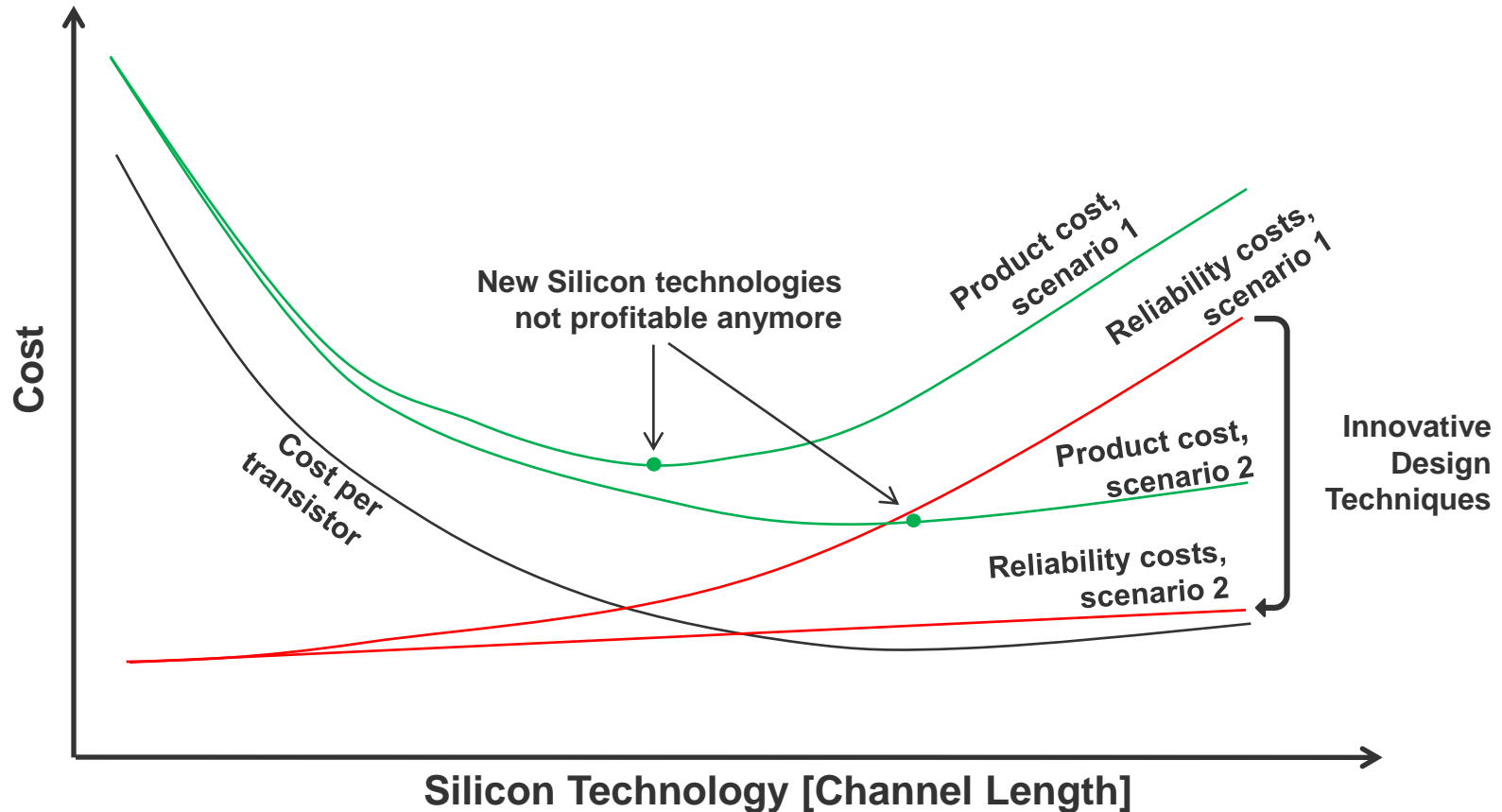
Source: Reliable Systems on Unreliable Fabrics, Todd Austin et al, IEEE Design & Test of Computers, 2008

Causes for Circuit Failure

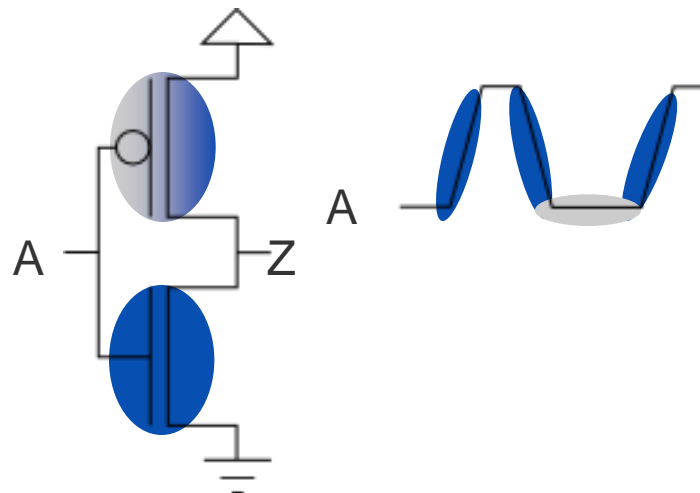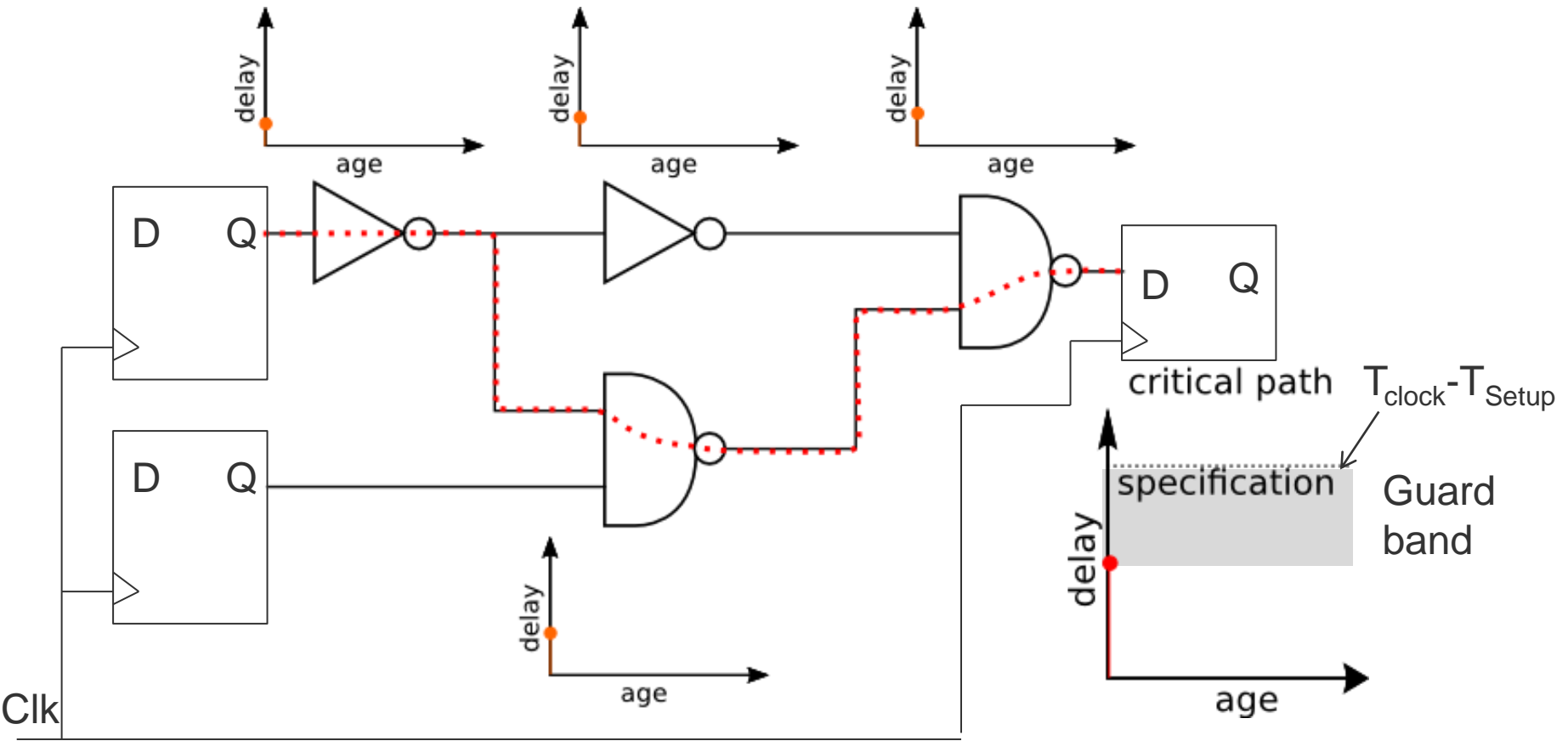| Permanent Errors	Transient Errors	Process Variations	Parameter drift
Time Dependent Dielectric Breakdown (TDDB), Electro-Migration (EM), …	Single Event Upsets (SEU) due to radiation, Cross talk, …	Variations in doping concentration densities, oxide thicknesses, diffusion depths,…	Negative Bias Temperature Instability (NBTI) Hot Carrier Injection (HCI)
Statistical treatment (What is the risk that an IC will fail?)	Statistical treatment (What is the risk that an error at the output occurs?)	Statistical treatment (SSTA: What is the Sigma and Mean)	Deterministic treatment (How large is the degradation?)

⬆ Timing Sign-Off ⬆

Dominant drift-related aging effects

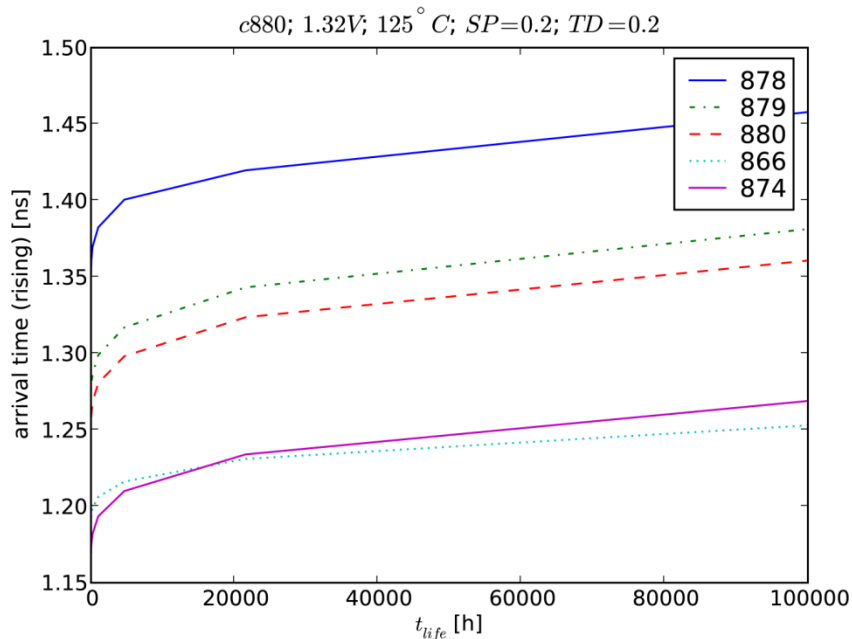|	**Negative Bias Temperature Instability (NBTI)**	**Hot Carrier Injection (HCI)**
Device	PMOS	PMOS & NMOS
Modeled by	Threshold voltage drift ΔV_{th}	Degradation of drain saturation current ΔI_{on}
Stress condition	Transistor in inversion	Transistor switches

Traditional timing sign-off

critical path

$T_{clock} - T_{Setup}$

Guard band

Timing sign-off considers aging (Aging analysis)
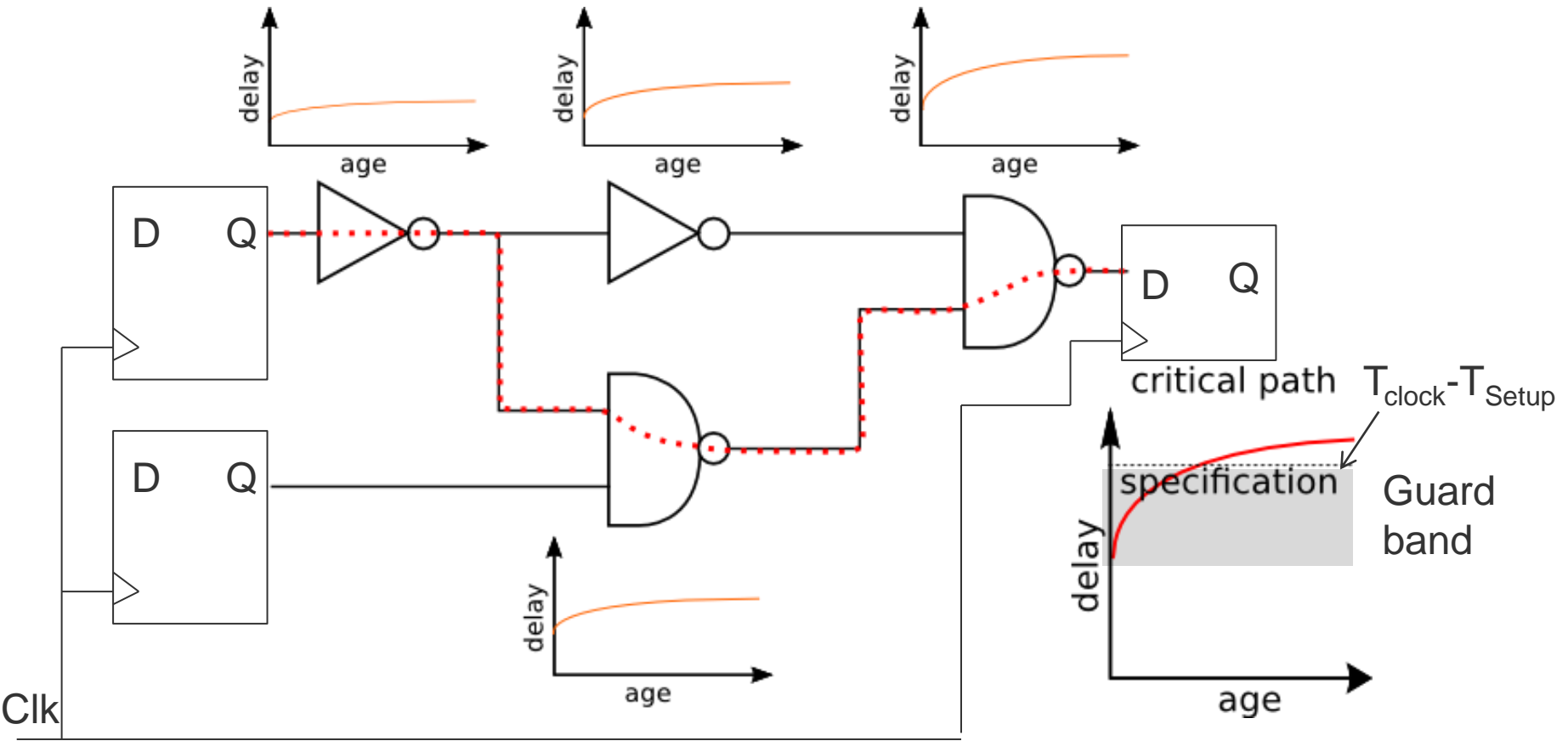
critical path

$T_{clock}-T_{Setup}$

Guard band

Clk

Output arrival times over lifetime

$c880; 1.32V; 125^{\circ}C; SP=0.2; TD=0.2$

- 90nm industrial cell library
- Output 866 and 874 change order: uncritical path can become critical due to aging

- Operating conditions: P_{nom}, 27°C, 0.9V
- Use profile: 125°C, 1.32V, 10y
- Workload by probabilistic method

Gate performance degradation given by parameter drift & gate sensitivity

90nm; 10a; 125°C

90nm; inverter; 1.2V; 27°C
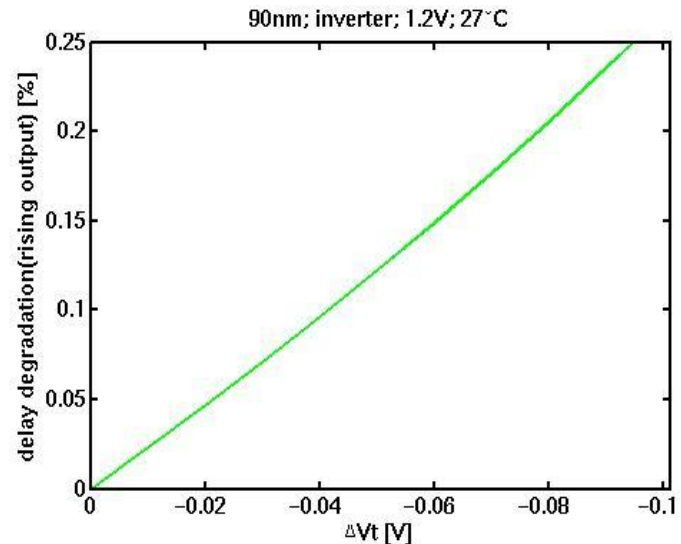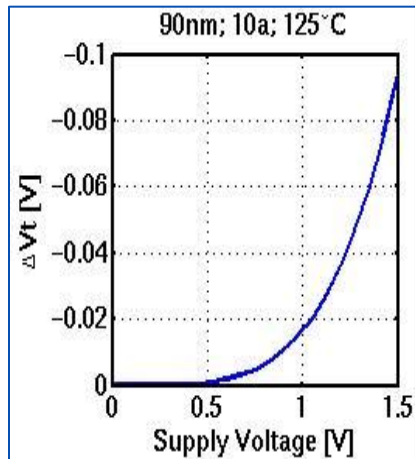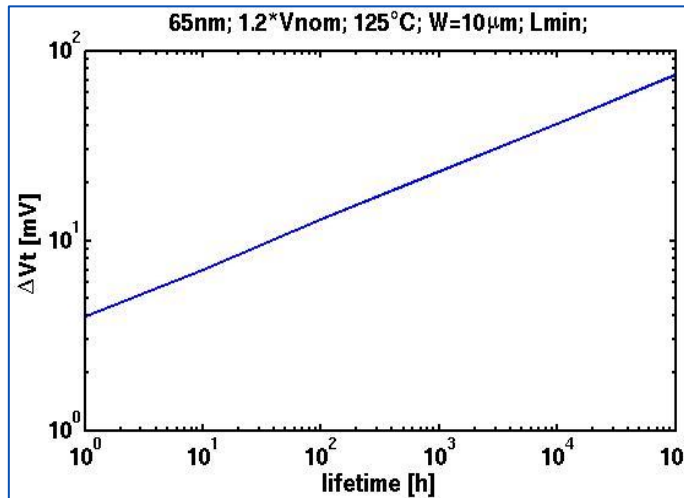
1. Calculate **parameter drift**

2. **Sensitivity** of gate properties

Degradation of gate performance (e.g. gate delay)

Logarithmic lifetime dependence

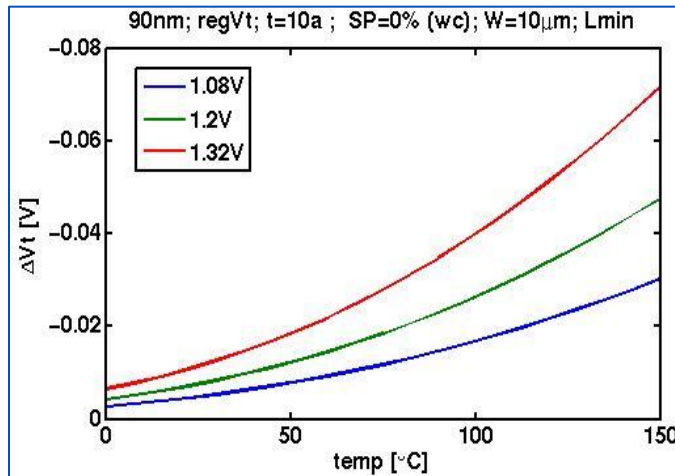### Drift over lifetime (DC stress)

65nm; 1.2*Vnom; 125°C; W=10μm; Lmin;

- Aging ⇨ Drift increasing with time
- Modeling degradation at End of Lifetime (EOL) is sufficient

- Circuit recovers in unstressed condition
- Never recovers to state before stress period

Drift over lifetime (Periodic stress)

ΔV_{th}
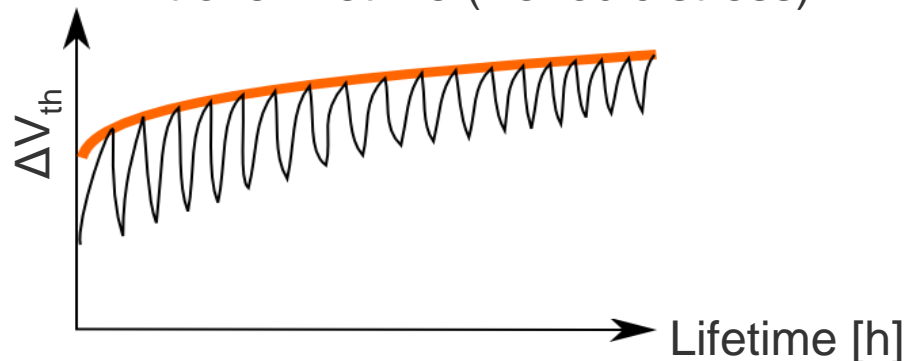
Lifetime [h]

Supply voltage and temperature affect drift & sensitivity

drift

90nm; regVt; t=10a ; SP=0% (wc); W=10μm; Lmin
- 1.08V
- 1.2V
- 1.32V

Lower Supply voltage:

V_{th}-drift ↓ and gate

sensitivity ↑

sensitivity

90nm; Inverter; T=85°C
- 0.9V
- 1.2V
- 1.47V

C65LP R09_SIVX020; V_{DD}=1.2V
- −40
- 27
- 85
- 100
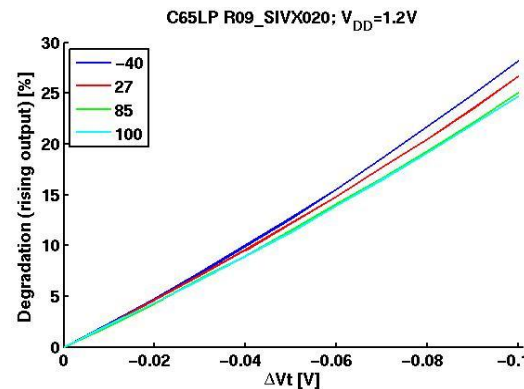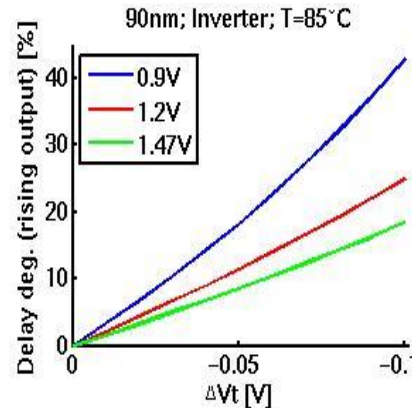
- Effective value ⇨ drift (value over lifetime)
- Current value ⇨ sensitivity

- Worst-case scenario: Stressed in $V_{DD,HIGH}$-Mode & operating in $V_{DD,LOW}$-Mode ⇨ high drift and high sensitivity

Workload: Signal Probability and Transition Density

- Signal probability (SP): Probability that signal has the logic value '1'

- SP=0.75

  t [ns]

- SP=0.5   TD=1

  t [ns]

- Transition density (TD): Average number of signal transitions/time unit

- SP=0.5   TD=0.5

  t [ns]

Drift is dependent on workload

- Workload = input signals/lifetime

- Input signals define stress condition

- Real signal:
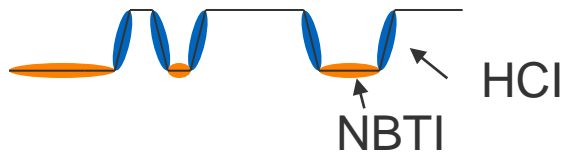
- Periodic signal with same signal probability SP & transition density TD

Drift over signal probability (SP) due to NBTI

- SP & TD for reliability analysis by:
  - Simulation (input vector!)
  - Probabilistic methods
  - Not avail. ⇨ worst case

Gate sensitivity for different technologies
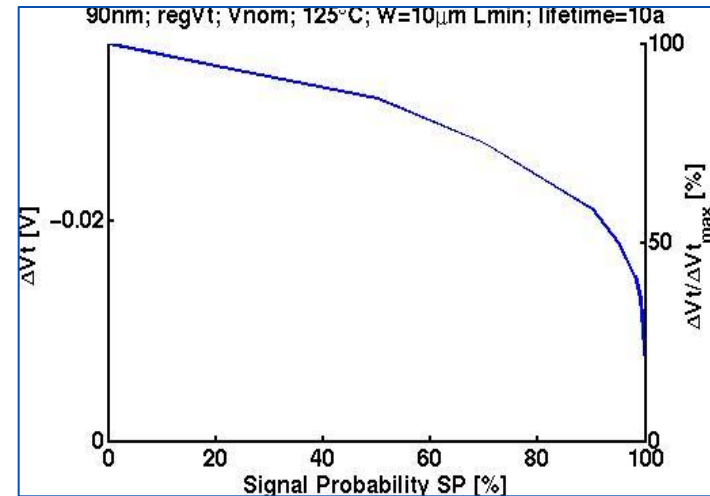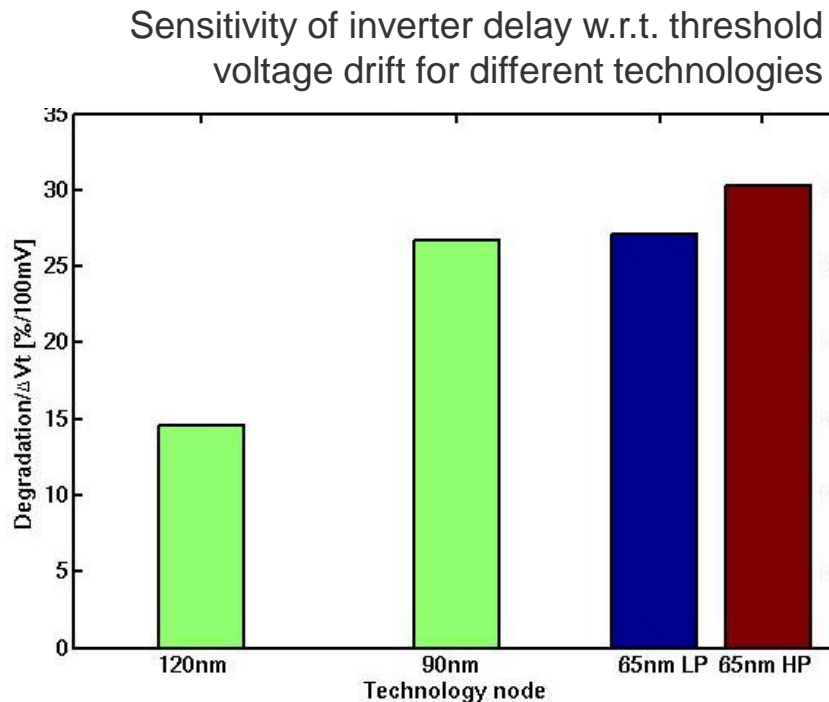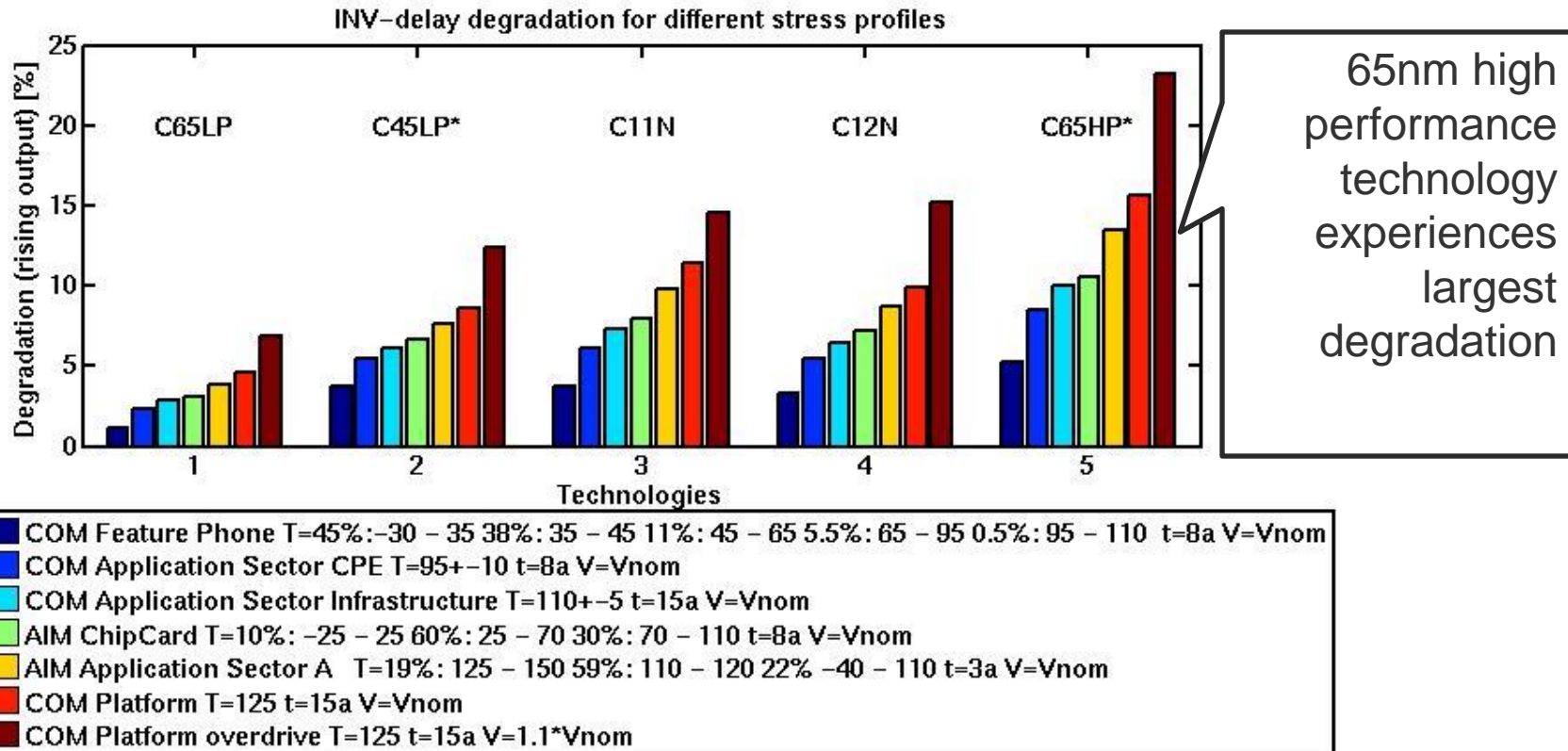
Sensitivity of inverter delay w.r.t. threshold voltage drift for different technologies

- Gates are more sensitive to a transistor parameter drift in newer technologies (because of lower supply voltage)

Technology trend:
Performance degradation for different stress profiles

INV−delay degradation for different stress profiles

65nm high performance technology experiences largest degradation

Legend:
- COM Feature Phone T=45%:−30 − 35 38%: 35 − 45 11%: 45 − 65 5.5%: 65 − 95 0.5%: 95 − 110 t=8a V=Vnom
- COM Application Sector CPE T=95+−10 t=8a V=Vnom
- COM Application Sector Infrastructure T=110+−5 t=15a V=Vnom
- AIM ChipCard T=10%: −25 − 25 60%: 25 − 70 30%: 70 − 110 t=8a V=Vnom
- AIM Application Sector A   T=19%: 125 − 150 59%: 110 − 120 22% −40 − 110 t=3a V=Vnom
- COM Platform T=125 t=15a V=Vnom
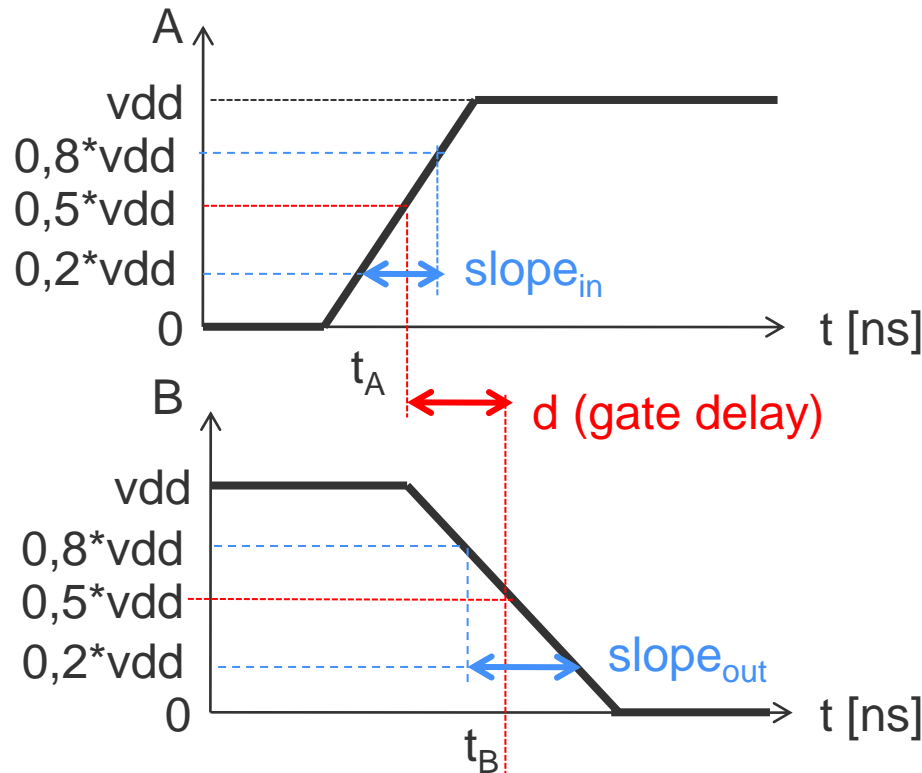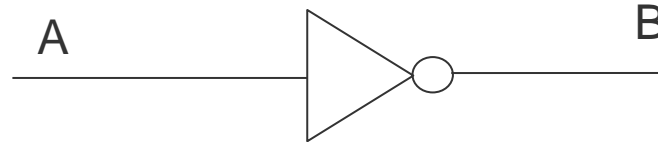- COM Platform overdrive T=125 t=15a V=1.1*Vnom

*C65LP netlist with exchanged transistor models

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Static Timing Analysis (STA) – Ramp Signal

Static Timing Analysis – Delay Models

A   B

A

t_A → t [ns]

B

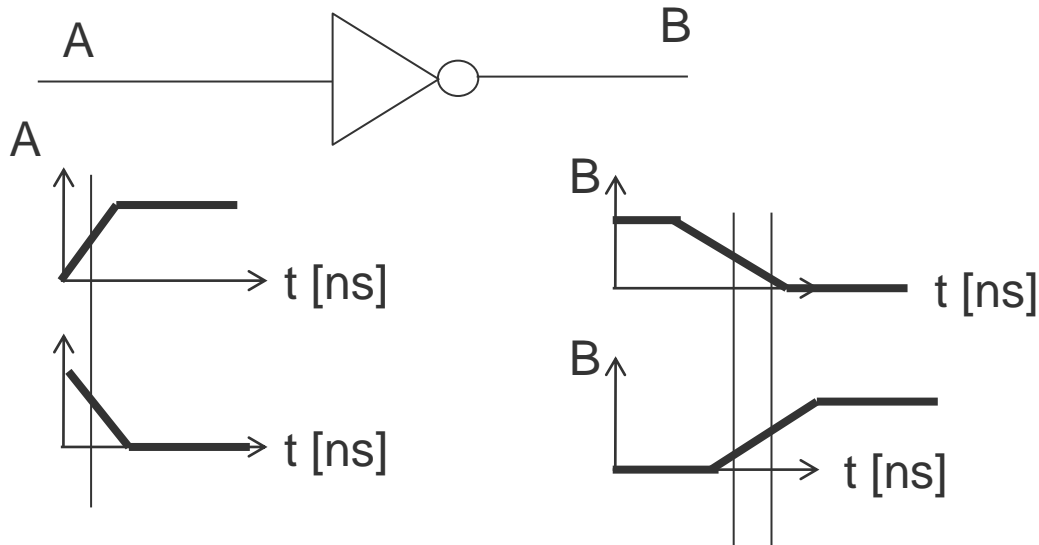t_B t_B → t [ns]
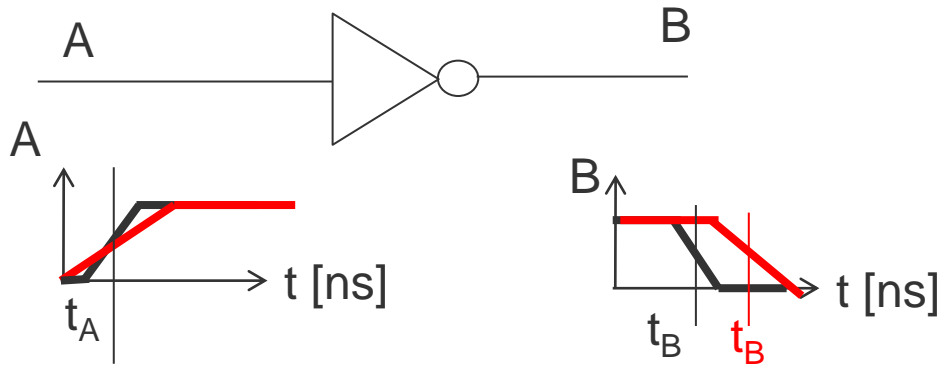
Gate delay d depends on input slope slope$_{IN}$
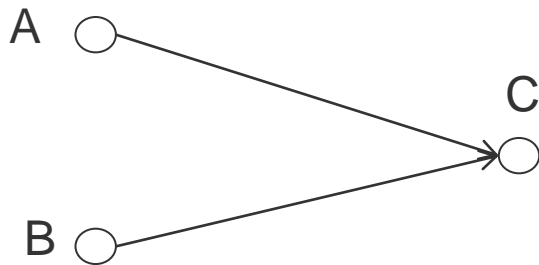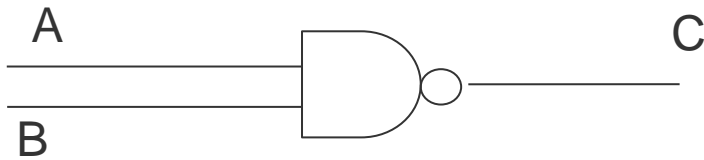
A

B

B

→ t [ns]
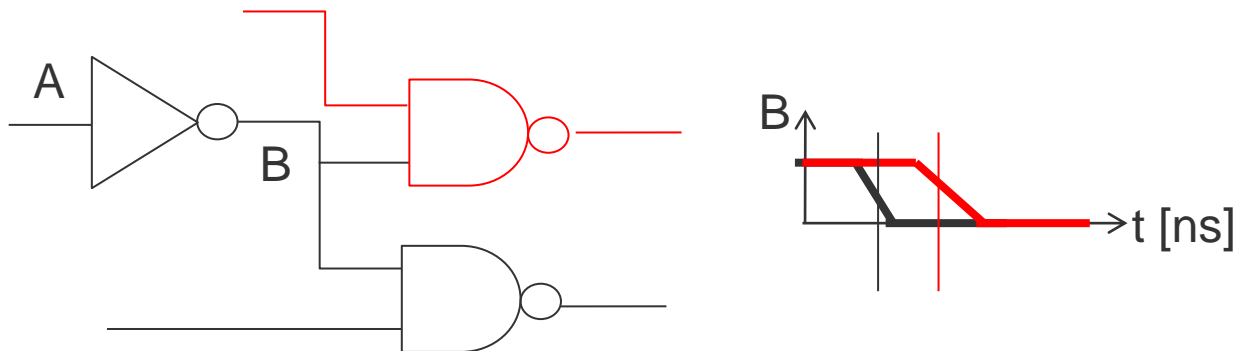
Gate delay d depends on gate loading

Static Timing Analysis – Delay Models

Gate delay different for rising/falling edges

Static Timing Analysis – Delay Models

A

C

B

A

C

B

- Gate delay different for different input pins
- Modeled by different edges in timing graph (TG)

- Delay from A to C is different to delay from B to C for same input signal

Static Timing Analysis (STA) - Propagation

Nonlinear Delay Model (Table based)

load: $C_{NAND,C}$

$slope_{IN}$: $slope_A$

INV,falling

$slope_{IN}$

load

d_{INV}

INV,falling

$slope_{IN}$

load

$slope_{out}$

$t_C = t_A + d_{INV,f}$

$$t_D = max(t_0 + d_{INV,f} + d_{NAND,CD,r},\ t_B + d_{NAND,BD,r})$$
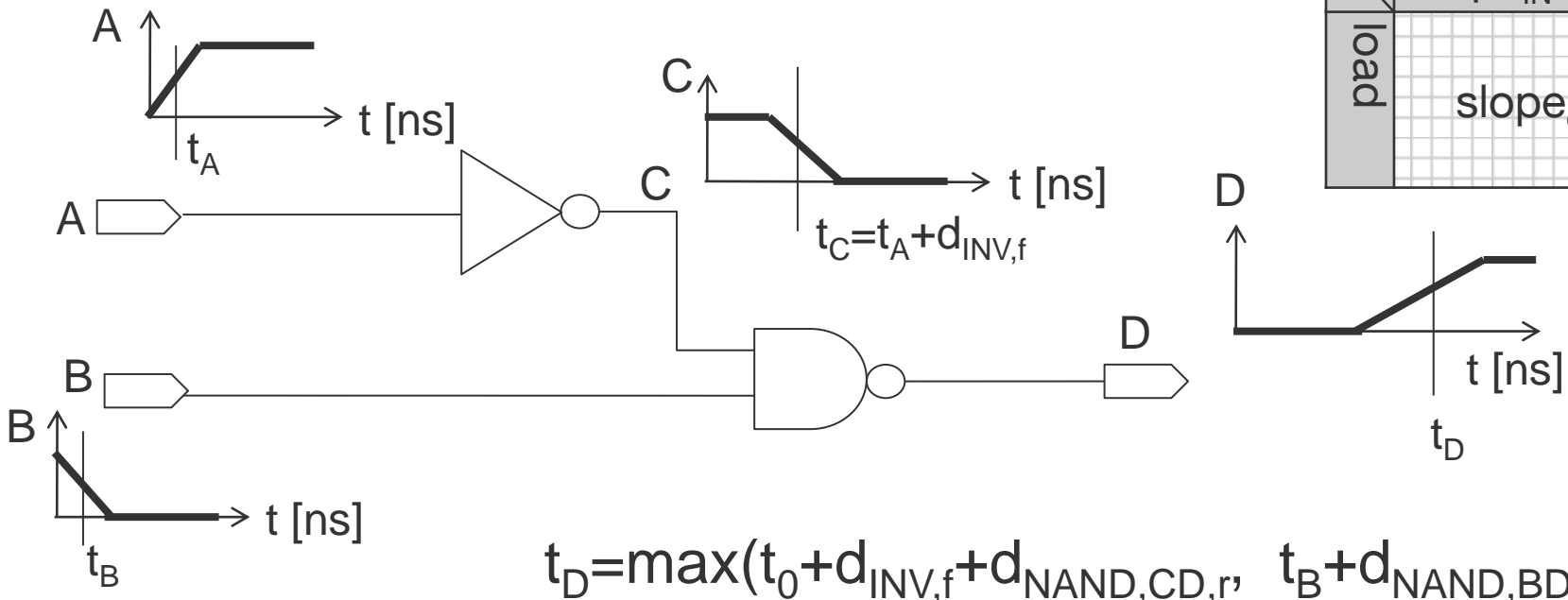
Aging-aware gate model required for aging analysis

Use profile (UP)
- operating conditions over lifetime

Workload
- signal probability SP
- transition density TD

Aged gate performances
- gate delay
- output slope
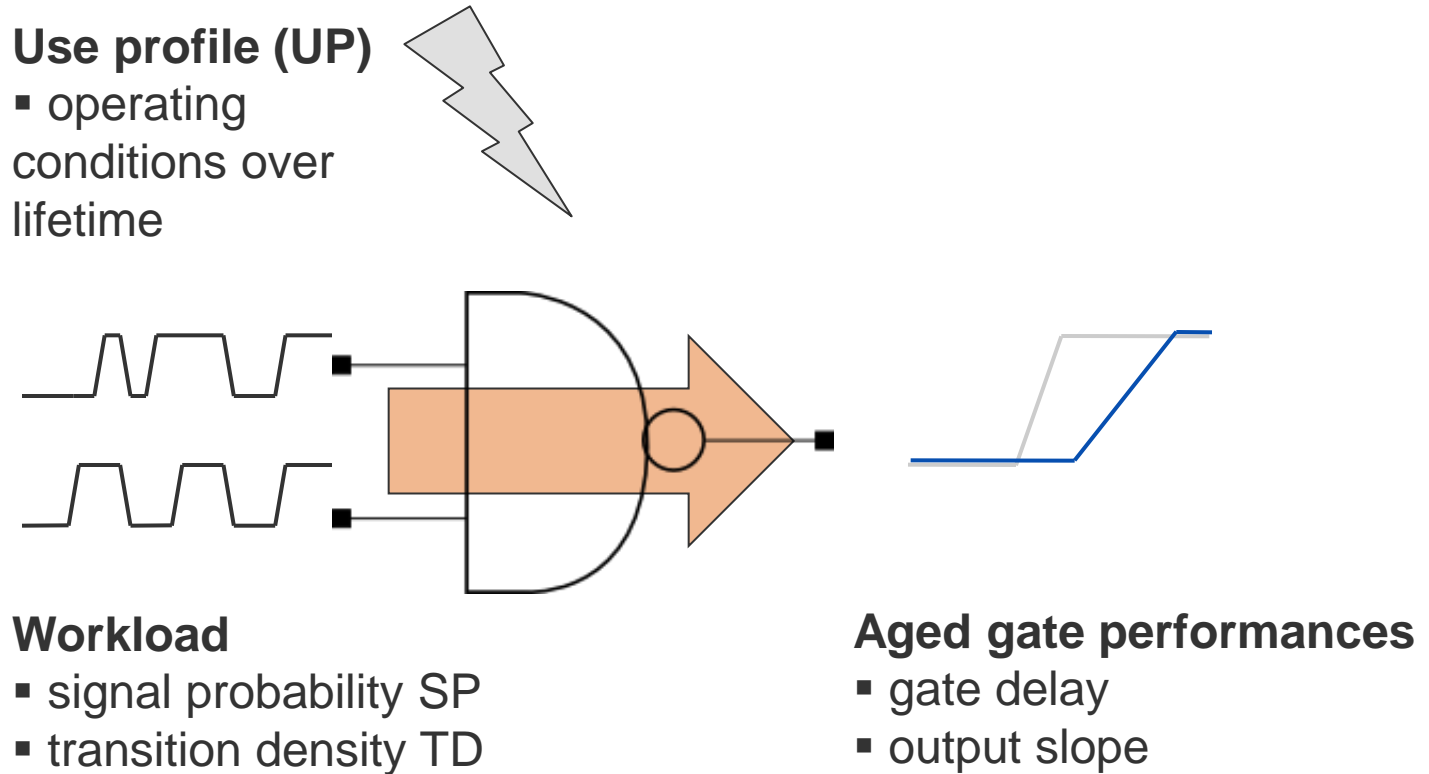
State of the Art - Table based approach
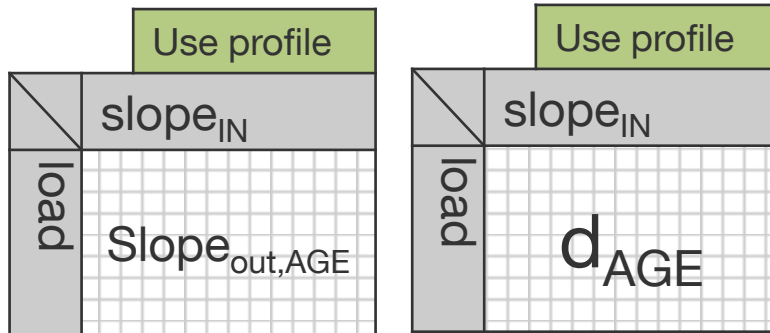
☹ New use profile ➜ library re-characterization

☹ Characterize gate for varying workload conditions

☺ Existing analysis flow can be reused
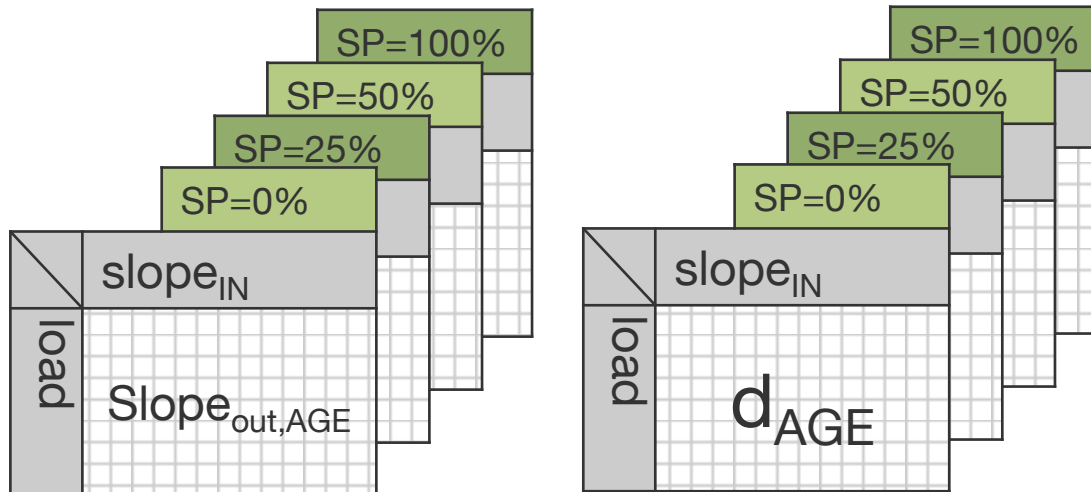
„GLACIER: a hot carrier gate level circuit characterization and simulation system for VLSI design", Wu et al., ISQED'00

State of the Art – Paul et al. (Alpha-power Law)

- Estimation of gate delay with α-power-law model:

d_{age}

d_0

ΔV_{th}

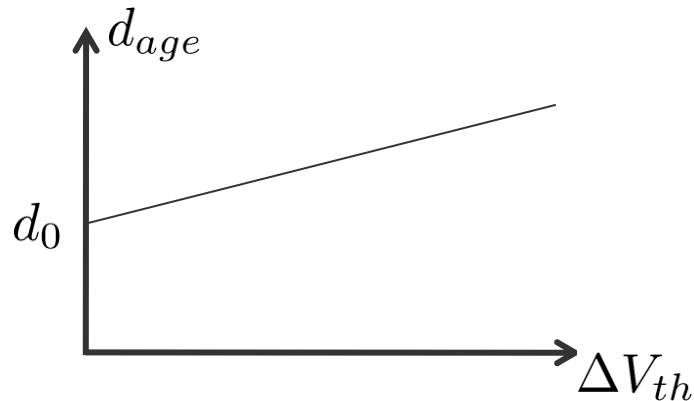$$d_{age} = d_0 + \frac{\partial d}{\partial V_{th}} \cdot \Delta V_{th}$$

with $\quad \dfrac{\partial d}{\partial V_{th}} = \dfrac{\alpha}{V_{gs} - V_{th,nom}} \cdot d_0$

- ☹ Only delay, no slope
- ☹ Only threshold voltage drift ΔV_{th}
- ☹ **One** ΔV_{th} for **all** transistors

- ☺ Use profile independent

"Temporal Performance Degradation under NBTI: Estimation and Design for Improved Reliability of Nanoscale Circuits", Paul et al., DATE'06

State of the Art – Sapatnekar & Cao

- Dependence on ΔV_{th} obtained during characterization:

$$d_{age} = d_0 + f\left(\Delta V_{th}\right)$$

- Radom signal represented as equivalent periodic signal described by Signal Probability (SP) (Sapatnekar)

- Long term prediction model for ΔV_{th} : closed form for upper bound of reaction-diffusion model (Cao)

☹ Only delay, no slope
☹ One ΔV_{th} for all transistors
☺ Use profile independent

NBTI

long term prediction model

time
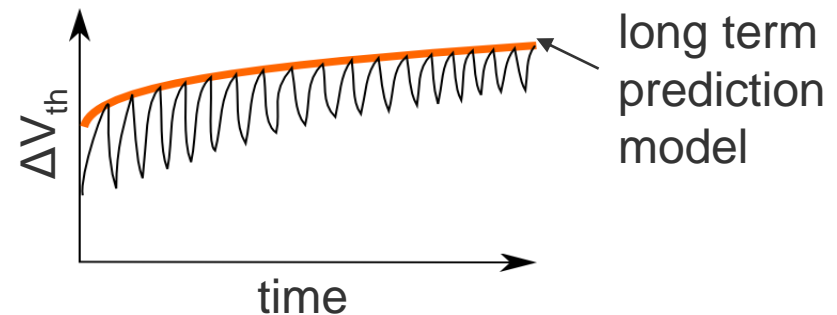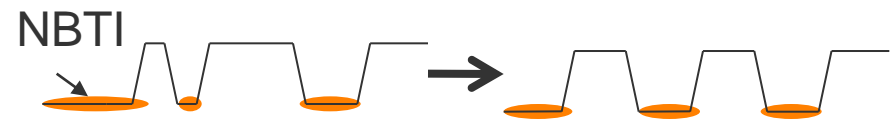
"An Analytical Model for Negative Bias Temperature Instability", Sapatnekar et al., ICCAD'06
"The impact of NBTI on the Performance of Combinational and Sequential Circuits", Cao et al., DAC'07

Comparison of approaches

	GLACIER	Paul	Sepatnekar	Cao	AgeGate*
NBTI (with recovery)		✓(✓)	✓(✓)	✓(✓)	✓(✗)
HCI	✓				✓
Individual transistor drifts					✓
Aged output slope					✓
Use profile independent model		✓	✓	✓	✓

*"Aging Analysis of Circuit Timing Considering NBTI and HCI", Lorenz et al., IEEE International On-Line Testing Symposium (IOLTS) 2009

Aging aware AgeGate gate model consists of 3 parts

Canonical gate model

Degradation equations

Structural information

Gate model provides aged gate performance for drifts

Canonical gate model

$$d_{Age} = d_0 + \sum_{m=1}^{M} (\chi_{m,NBTI}^{d} \Delta V_{th,m} + \chi_{m,HCI}^{d} \Delta I_{on,m})$$

$$slope_{out,Age} = slope_{out,0} + \sum_{m=1}^{M} (\chi_{m,NBTI}^{s} \Delta V_{th,m} + \chi_{m,HCI}^{s} \Delta I_{on,m})$$

M : # of transistors m

$\chi_{m,p}^{x}$: sensitivity coefficients

Degradation equations

Structural information

Drifts calculated by degradation equations

Canonical gate model
Degradation equations

- NBTI: $\Delta V_{th,m} = f(\mathbf{UP}, t_{\text{stress,NBTI,m}}, W_m, L_m)$
- HCI: $\Delta I_{on,m} = f(\mathbf{UP}, t_{\text{stress,HCI,m}}, W_m, L_m)$

$$t_{\text{stress,NBTI,m}} = P_{NBTI,m} \cdot t_{\text{life}}$$
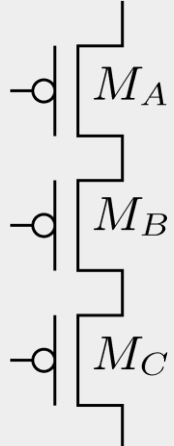$$t_{\text{stress,HCI,m}} = P_{HCI,m} \cdot t_{\text{life}}$$

$P_{NBTI(HCI),m}$: Probability that transistor m in stress cond.

$\mathbf{UP}$: use profile: Temp, Vdd

W_m, L_m : transistor sizes

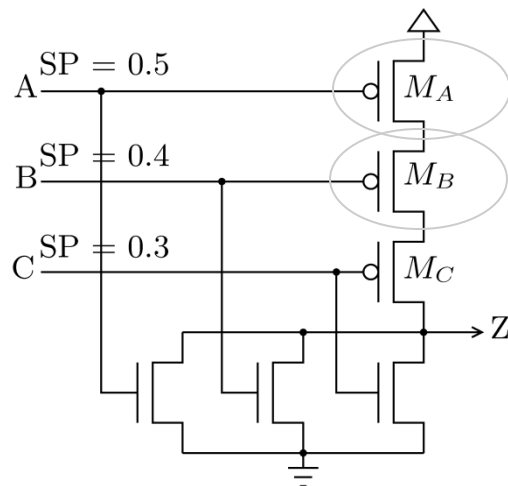| Structural Information |
|:---:|

Structural information needed for drift calculation

Canonical gate model

Degradation equations

Structural information

- Transistor sizes

- Transistor stack structure

M_A

M_B

M_C

Calculating stress probability for NBTI

NBTI stress condition for transistor M:

- 0V applied to gate contact of M
- Source contact of M has to be at Vdd

NOR3

Example:

- M_A stressed $\Leftrightarrow$ A at "0"

- M_B stressed $\Leftrightarrow$ Signals B & A at "0"
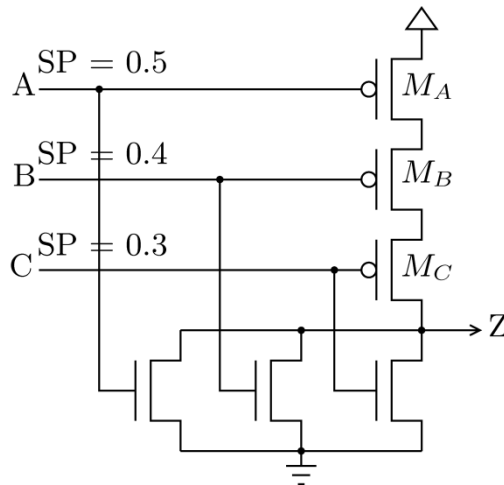
Calculating stress probability for NBTI

Stress condition for transistor M_B:

- 1-SP_B: logic "0" applied to gate contact of M_B

$\Longrightarrow 1 - SP_B = P(M_B \text{ "in Inversion"})$

- 1-SP_A: logic "1" applied to source contact of M_B

$\Longrightarrow 1 - SP_A = P(M_A \text{ in "Inversion"})$

NOR3

For independent signals

$$P_{\text{NBTI,B}} = P(\text{A is } '0' \wedge \text{B is } '0')$$
$$= (1 - SP_A) \cdot (1 - SP_B)$$

For dependent signals: Worst-case assumption

$$P_{\text{NBTI,B}} = P(\text{A is } '0' \wedge \text{B is } '0')$$
$$= \min((1 - SP_A), (1 - SP_B))$$

Aging analysis flow
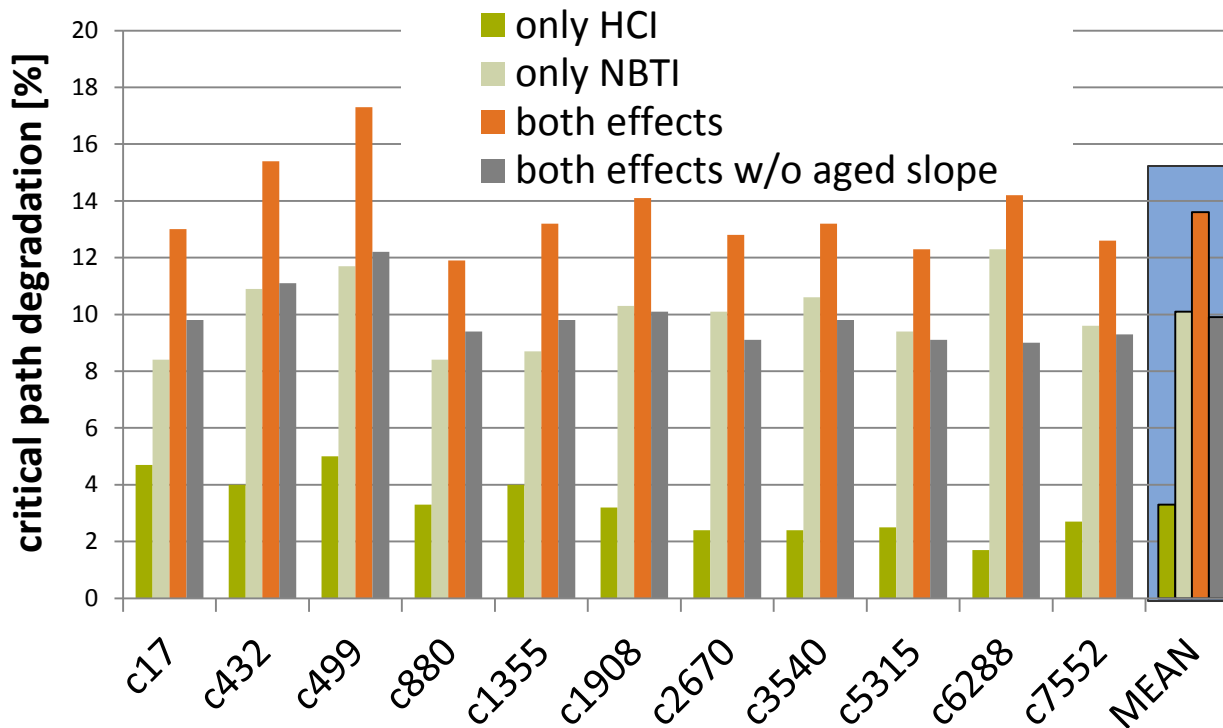
Use profile specification

Workload determination
- Logic simulation
- Probabilistic method
- Specification of worst-case values

Timing analysis
- Compute stress probability
- Compute parameter drift
- Compute gate performances

Degradation of critical path delay for ISCAS'85 benchmark circuits

- Industrial 90nm cell library
- Use profile: 125°C, 1.32V, 10y
- Measurement conditions: 27°C, 0.9V
- Worst-case analysis (SP=0 and TD=2 for all nets)
- Runtime: 35s for c7552

- Both effects are relevant
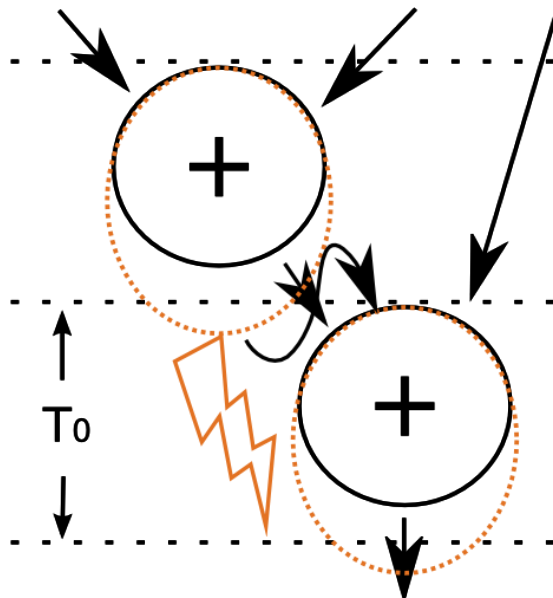- Not considering aged output slope → 24% underestimation

Comparison: w and w/o individual transistor drifts
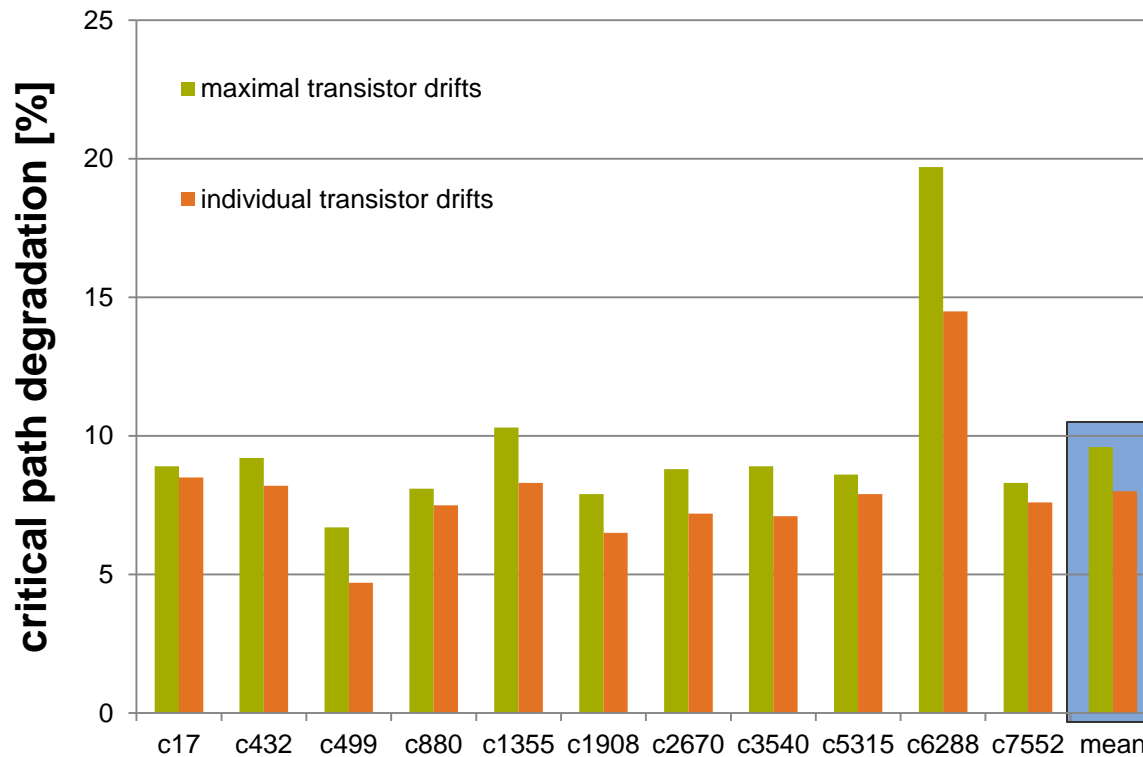
- Workload estimation with probabilistic method (*SP*=0.5 and *TD*=0.4 at all inputs)

▪ w/o individual transistor drifts ➔ degradation 20% overestimated

Timing Model on Register Transfer Level (RTL)

- RTL: Mapping of logical/arithmetical operations to time slot of duration of the clock period T_0
- Example: Adder operation must finish in one clock period
- Aged circuit *might* fail because operation takes longer than T_0

Aging-aware timing model (TM) at RTL enables:

- Considering impact of aging on system early in design process
- Quick performance determination at system level
- Design space exploration

Timing models on RTL
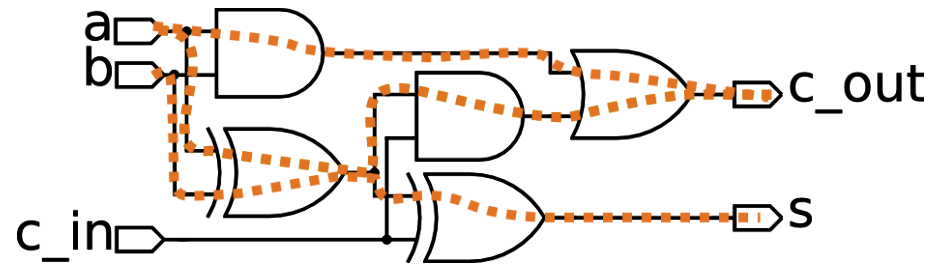
- Functional unit delay determined by critical path delay
- **w/o aging: one critical path**
- **with aging: multiple possible critical timing paths**

Proposed aging-aware RTL Timing Model*

Idea: Reduced timing graph (TG) that just contains **possible critical paths (PCP)**

A possible critical path (PCP) is the critical path of a degraded circuit for a defined combination of temperature T, supply voltage V, workload of the input signals and lifetime t.
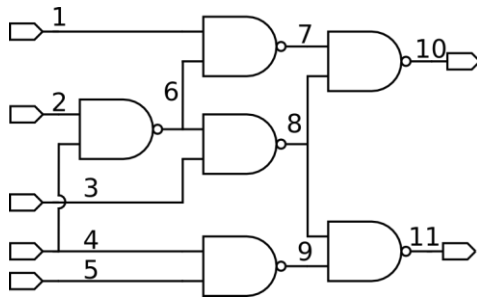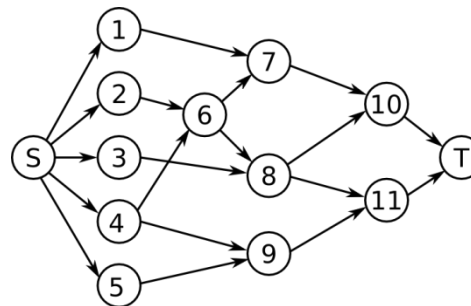
schematic   timing graph   reduced timing graph

- As accurate as timing analysis on gate level
- Speed-up due to reduced TG

"Aging model for timing analysis at register-transfer-level", Lorenz et al., TAU 2010

Aging-aware gate model needed for generation/evaluation of RTL Timing Model

operating conditions over lifetime & workload
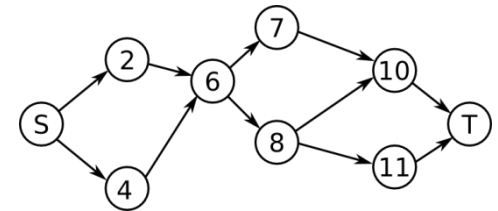
A $\longrightarrow\!\triangleright\!\circ\!-\!$ Z

d_0

d_{age}

A $\circ\!\!-\!\!\longrightarrow\!\!\circ$ Z

$[d_0, d_{age,max}]$
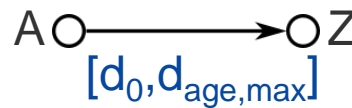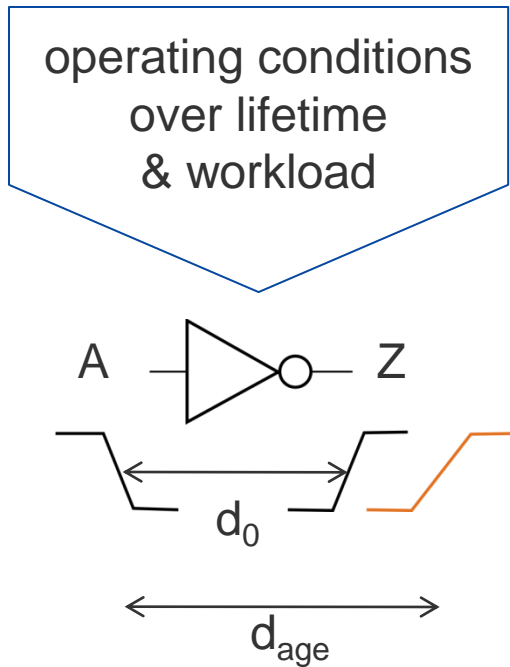
- Approach independent of used gate model

- Interval for gate delay because actual gate delay unknown during characterization

d_0: fresh gate delay

d_{age}: aged gate delay

Reduction of the Timing Graph

- Identification of elements that are not part of a possible critical path:
  1. Block-based reduction step
  2. Path-based reduction step
  3. Reconvergent fan-out reduction step

- Validity region has to be specified:
  - max lifetime
  - max temperature
  - max supply voltage
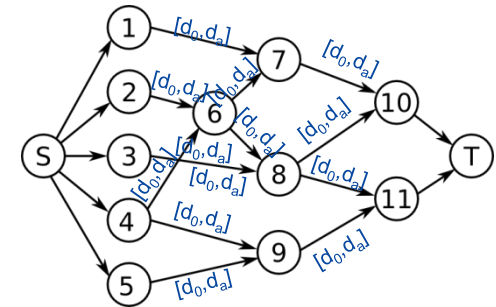
1. Block-based reduction step

"Sum" and "max":

$$\texttt{sum}([A_l, A_u], [B_l, B_u]) = [A_l + B_l, A_u + B_u]$$

$$\texttt{max}([A_l, A_u], [B_l, B_u]) = [\max(A_l, B_l), \max(A_u, B_u)]$$

"Lesser than":

$$[A_l, A_u] < [B_l, B_u] = A_u < B_l$$

[10,13]   A

[13,14]   B

[8,10]   C

[3,4]

[1,2]

Z

[14,17] =
max([13,17],
  [14,16],
  [9,12])
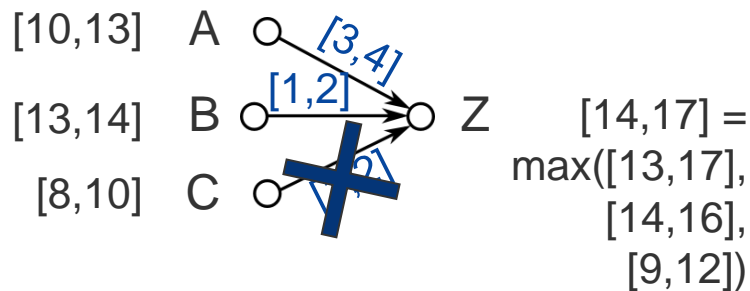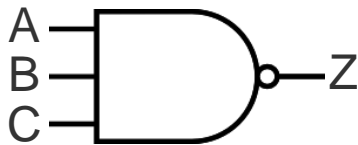
- Static timing analysis with intervals

2. Path-based reduction step

- Delay of possible critical paths > critical path delay of fresh circuit !

3. Reconvergent fan-out reduction step

full paths

$D(P_1)=[3,6]$

$D(P_2)=[2,4]$

disjoint sub-paths
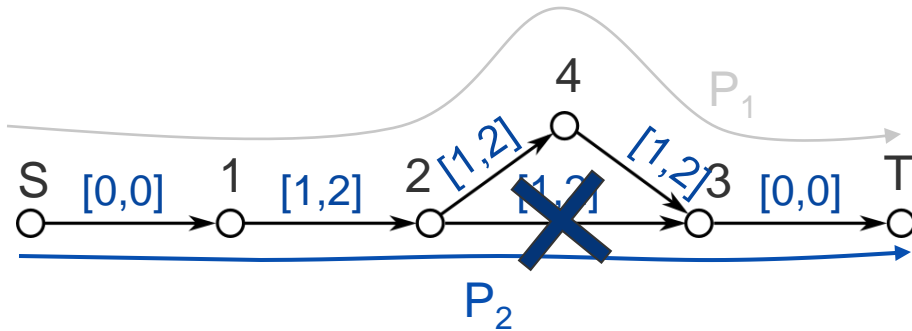
$D(P_1 \backslash P_2)=[2,4]$

$D(P_2 \backslash P_1)=[1,2]$

- Checks whether the faster of two sub-paths is also a possible critical path

Results

- RC-adder, CLA-adder, ISCAS'85 benchmarks
- 90 nm industrial cell library

- $$\text{Reduction (ratio)} = \frac{\text{removed nodes (edges)}}{\text{nodes (edges) of original TG}}$$
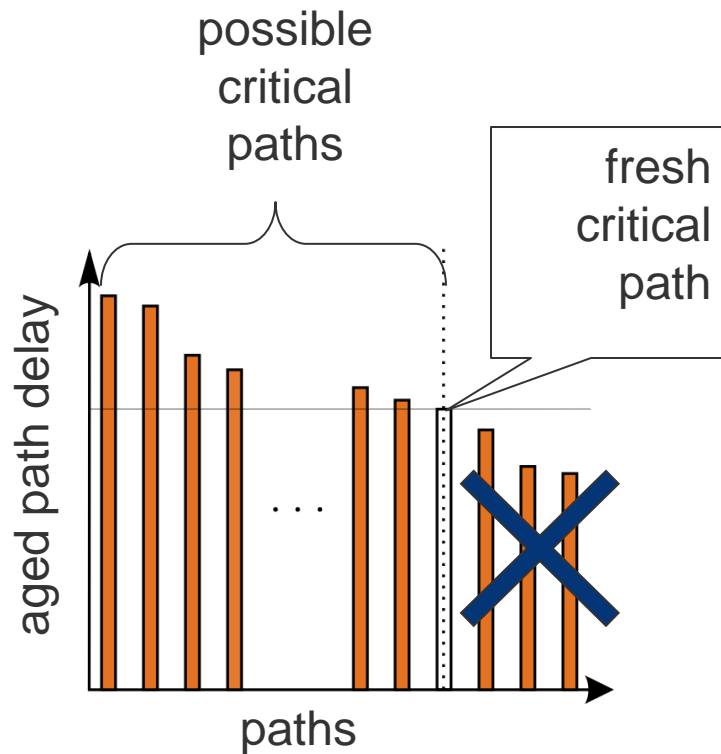
- Two validity regions specified:
    - Region 1: 100°C; 1.2V; 5y $\rightarrow$ max ΔV_{th} = 8%
    - Region 2: 125°C; 1.32V; 10y $\rightarrow$ max ΔV_{th} = 17%

original TG
C17(ISCAS'85)

red. TG
region 1

red. TG
region 2
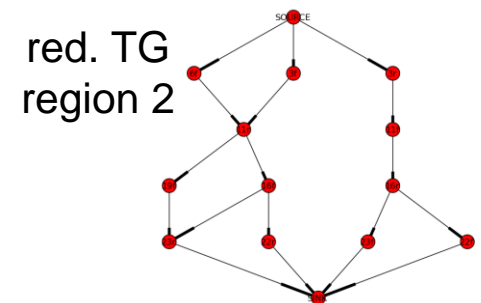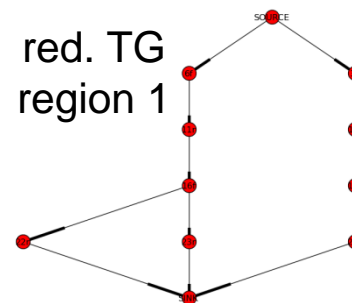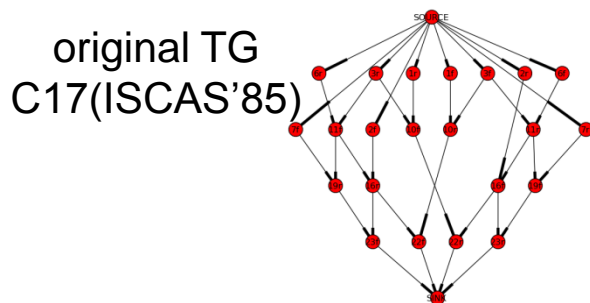
Achieved reduction ratios
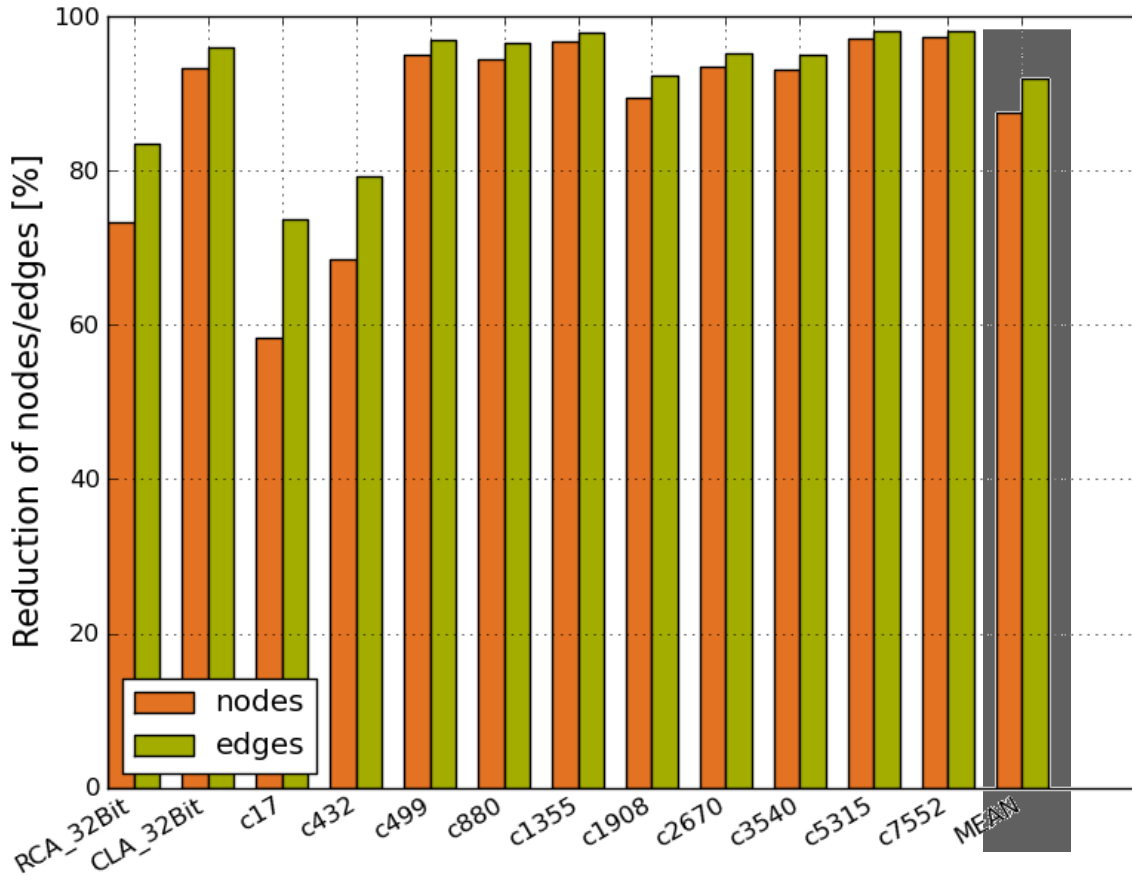
- Mean reduction:
  88% for nodes
  92% for edges

- Speed-up compared
  to timing analysis on
  gate level:
  56x (mean 25x)

- Characterization
  time: < 1min
  (except c432: 7min)

Agenda

- Institute for Electronic Design Automation at TUM
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    - Aging Effects on Digital Circuits
    - Aging Analysis on Gate and Register-Transfer Level
    - **Aging Monitors**
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    - Measuring robustness
    - Robustness as a probability
    - Robustness of Digital Circuits

Impact of workload on degradation (c880)
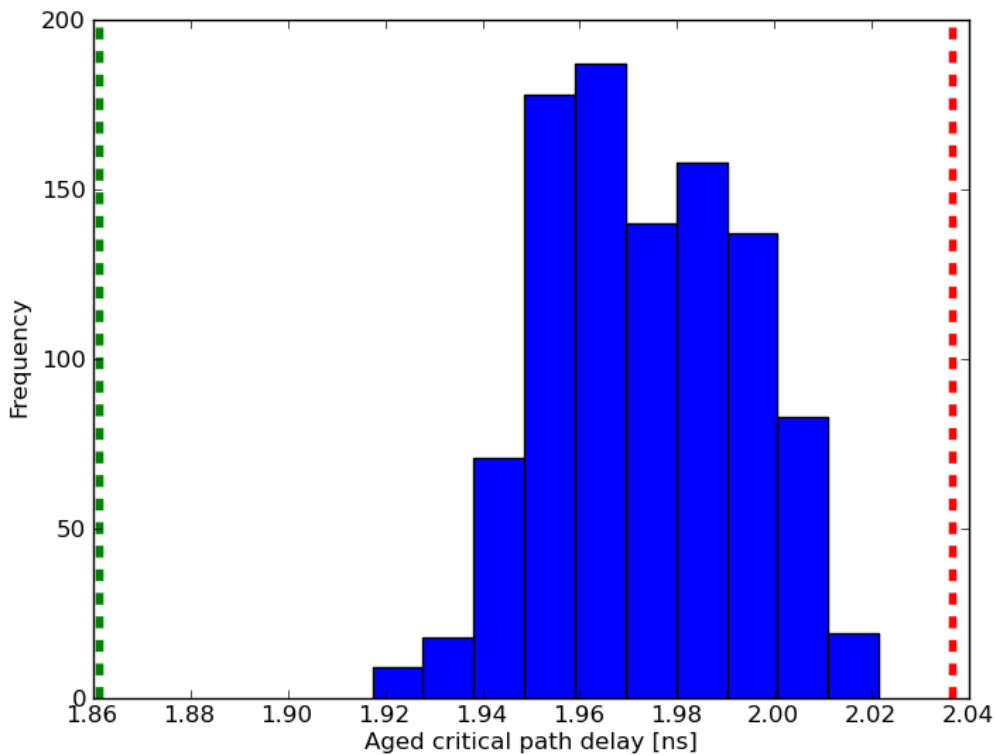
MCA over SP (workload) at inputs

Workload and operating conditions are unknown:

- Worst-case design
- Better: Monitor and react

Ways to monitor aging

- Single device monitors
  - Measure threshold voltage drift
  - Hard to correlate to circuit performance
- Generic test structure (e.g. inverter ring oscillator)
  - Measure oscillating frequency
  - Neglects workload impact
- Circuit replica (e.g. critical path replica)
  - Measure delay/oscillating frequency
  - Neglects workload impact
- Delay fault test
  - Measure delay of current critical path
  - Only safe way: **Workload impact considered**
  - Operation must be paused

Requirements for delay fault monitor

- Built-In Self Test (BIST)
- (Enhanced) scan design
- Test vectors for all possible critical paths

Possible critical path (PCP):

A possible critical path (PCP) is the critical path of a degraded circuit for a defined combination of temperature T, supply voltage V, workload of the input signals and lifetime t.

Enhanced scan design
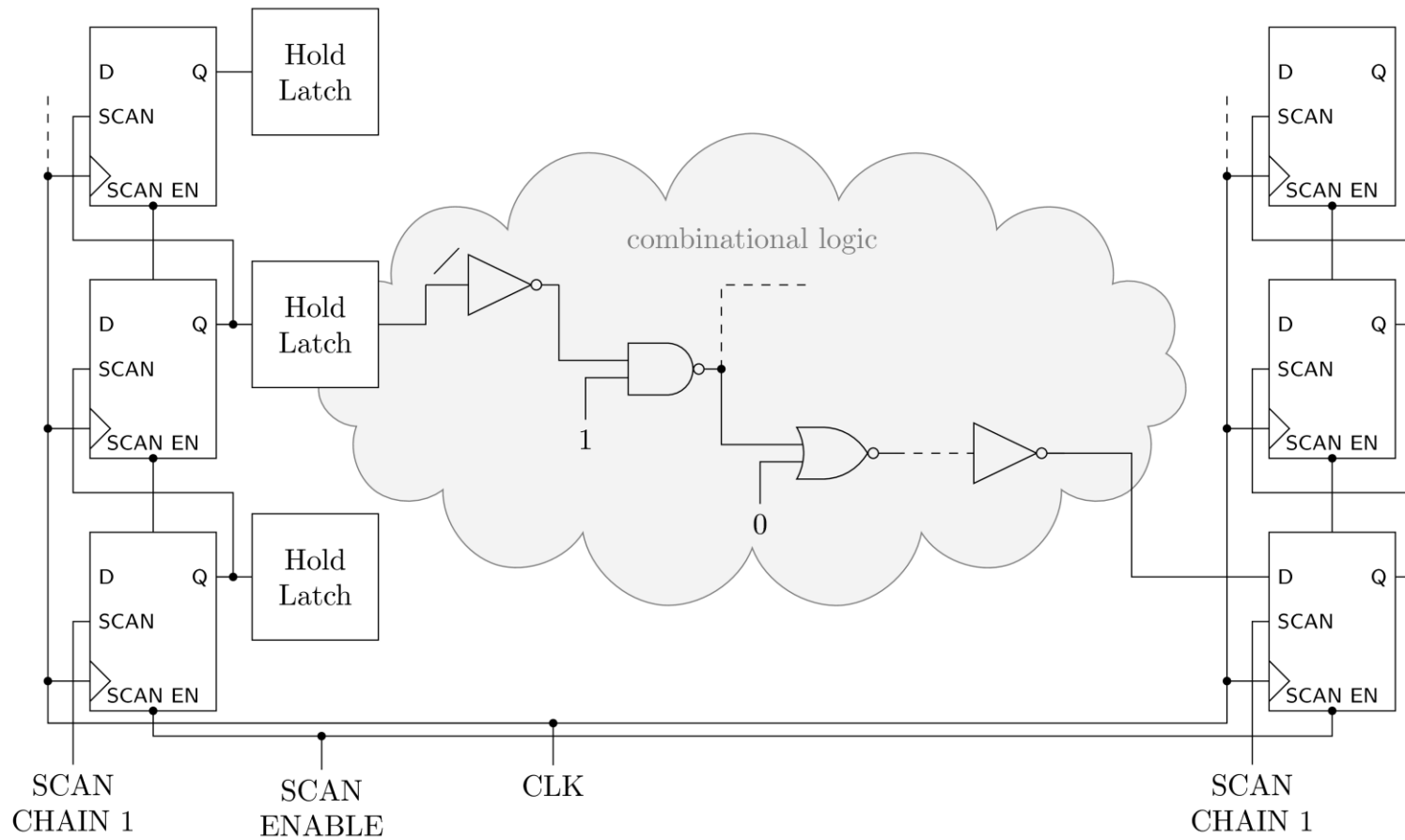
Ways the system can react

- Disable degraded circuit (e.g. one core of multi-core processor)

- Reduce clock frequency

- Increase supply voltage (Caution: accelerates aging)

- Replace degraded circuit by redundant one (degraded circuit can recover)

- Use degraded circuit for uncritical tasks (probabilistic CMOS)

State of the art: Path selection approaches (Test vectors for all possible critical paths)

- Nominal case:
  - "On Path Selection in Combinational Logic Circuits", Li, TCAD'89
  - "Finding a small set of longest testable paths that cover every gate", Sharma, ITC'02
- Process variation:
  - "Longest-path selection for delay test under process variation", Lu, TCADICS'05
  - "Statistical Path Selection for At-Speed Test", Zolotov, TCADICS'05
- Aging:
  - "Testing for transistor aging", Baba, VTS'09

Identifying PCPs

schematic   timing graph   reduced timing graph
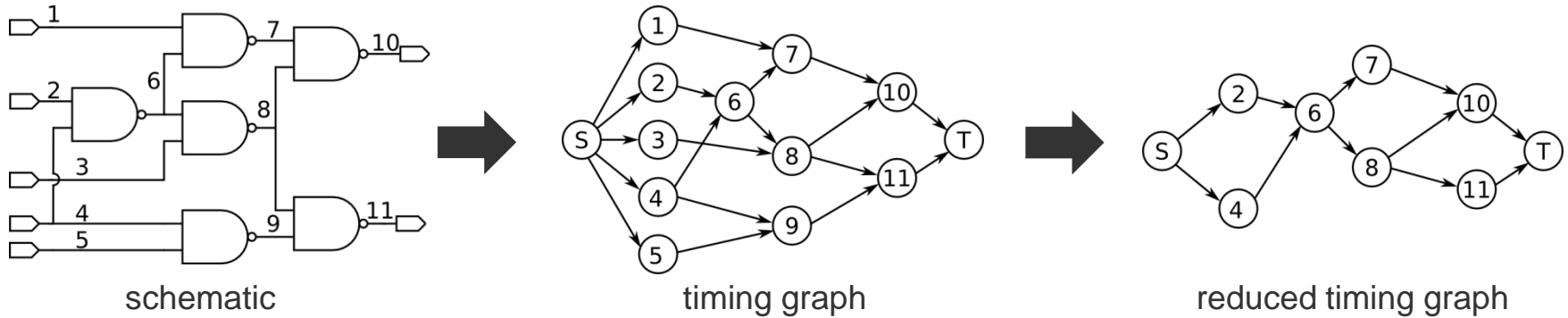
Basic idea: Reduced timing graph (TG)
- Gate delays modeled as intervals
- Remove edges & nodes not part of a possible critical path

Results

- ISCAS benchmark circuits
- Inverter, NAND and NOR gates from 90nm industrial cell library
- Operating conditions over lifetime:
  - Supply voltage: 1.32V
  - Temperature: 125°C
  - Lifetime: 10y
- Only NBTI

Possible Critical Paths (PCPs)

Circuit	#Paths	#PCPs [Baba]	Factor [Baba]	#PCPs [Ours]	Factor [Ours]
c17.v	18	3	6 x	3	6 x
c432.v	123652	157	788 x	157	788 x
c499.v	452608	1487	304 x	375	1207 x
c880a.v	16956	98	173 x	74	229 x
c1355.v	522368	3376	155 x	2224	235 x
c1908.v	1536434	4596	334 x	2091	735 x
c2670a.v	31286	21	1490 x	21	1490 x
c3540a.v	4248254	15276	278 x	1345	3159 x
c5315a.v	738816	1568	471 x	899	822 x
c7552.v	448564	3173	141 x	522	859 x
MEAN			**414 x**		**953 x**

- Mean reduction of paths: 953x (414x [Baba])

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  – Aging Monitors
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  – **Measuring robustness**
  – Robustness as a probability
  – Robustness of Digital Circuits

Reliability and Robustness

- **Reliability:**
  - A circuit is reliable, if it has a high probability to operate correctly according to its specification during its lifetime.
  - Specifications covers customers use cases.

- **Robustness:**
  - A circuit is robust, if it has a high probability to operate correctly even under conditions outside the specification during its lifetime.
  - Specification does not cover all possible use cases.
  - Safety critical applications in hard-to-predict enviroments.
  - Investigate complete range of operating conditions, in which circuits operate correctly -> Allows comparison of different implementations.

What's the use of measuring robustness?

- Designers can choose between different implementations of a circuit depending on the specification and the mission profile, e.g., temperature over lifetime.
- Possible optimization techniques

System view

$$\pi^{\mathbf{nom}} \quad , \Pi$$

$x(t)$ → f → $y(t)$

$$\phi^{\mathbf{nom}} \quad , \Phi$$
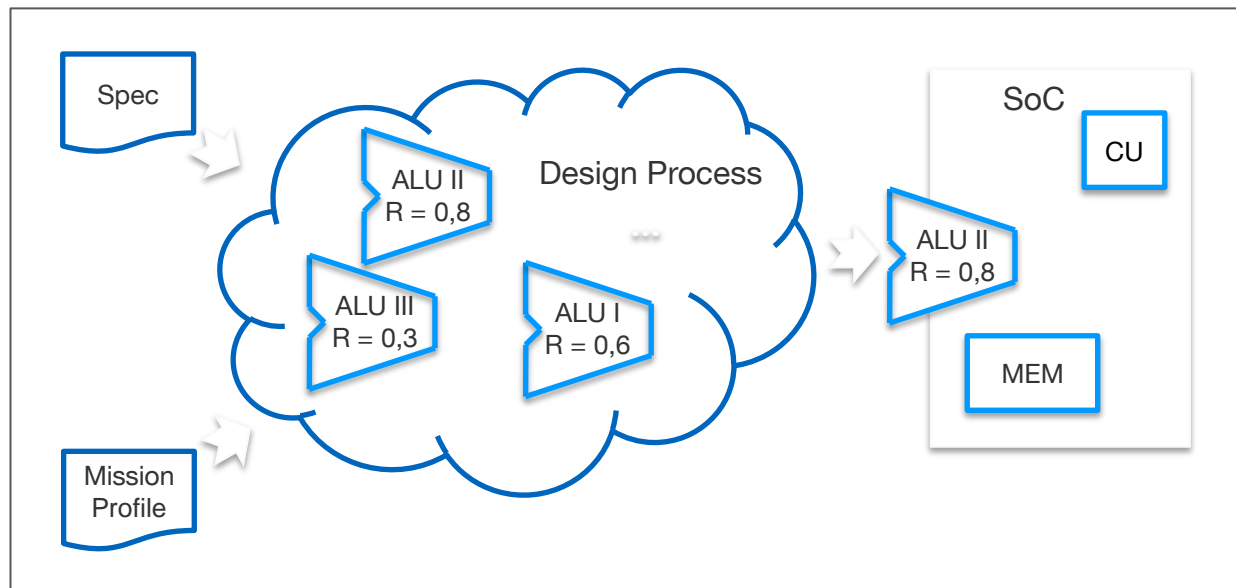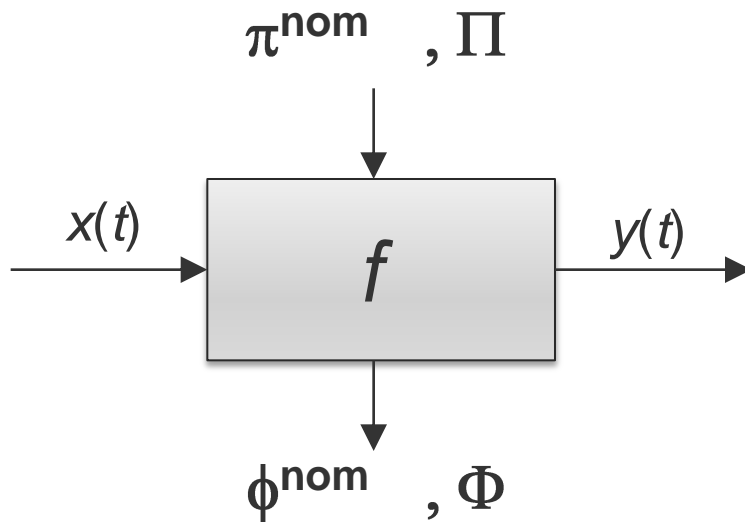
Example
- f : channel
- Π : external noise
- Φ : bit error rate

- Functionality: system transforms inputs → outputs

- Additional "input": operating conditions
  - nominal value, $\pi^{\mathbf{nom}}$
  - deviation around nominal conditions, perturbation Π

- Additional "output": generation / guarantee of properties, $\phi^{\mathbf{nom}}$ and Φ

Specification of required properties

Axis labels: ϕ_2, ϕ_1, Φ_A, Φ, Φ_B, ϕ_2^{max}, ϕ_2^{min}, ϕ_1^{min}, ϕ_1^{max}
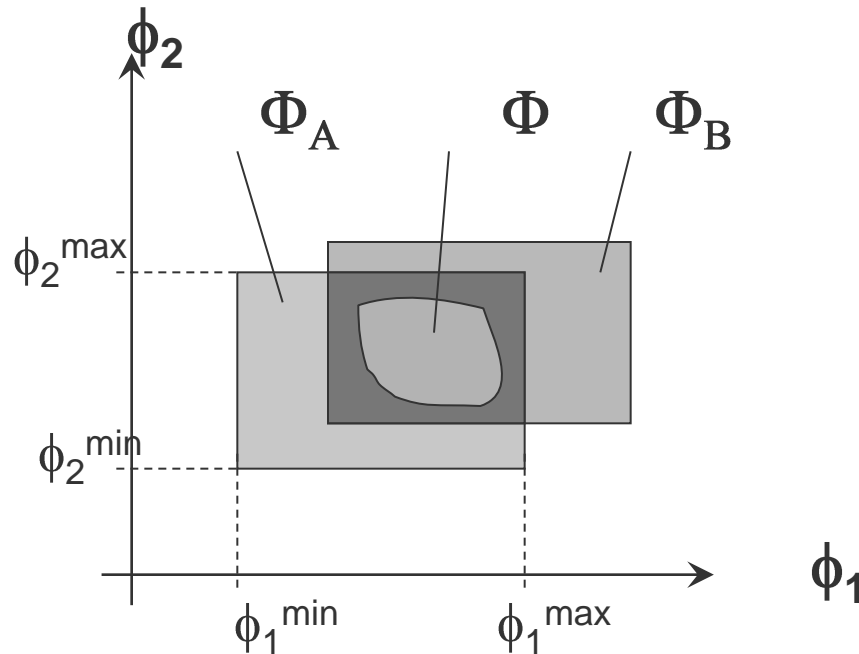
- Application A requires Φ_A

- Application B requires Φ_B

- A chip that supports A and B must meet both, Φ_A and Φ_B

- The chip specification may further narrow down the properties Φ (robustness margin)

Specifies *what* is robust
(properties Φ of system f)

Specification of tolerated operation conditions
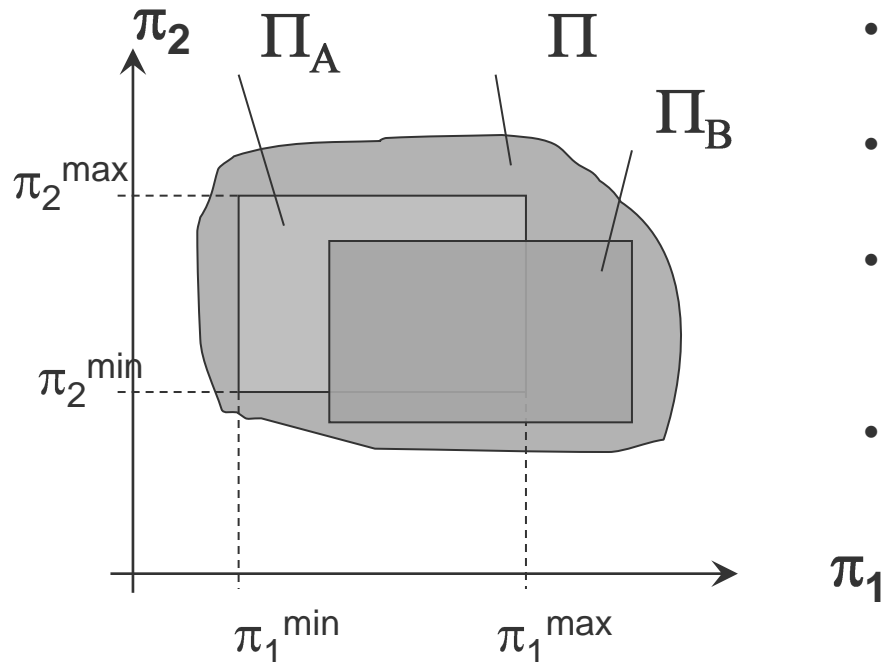
- Application A must tolerate Π_A

- Application B must tolerate Π_B

- A chip that supports A and B must tolerate Π_A or Π_B

- The chip specification may further extend the operating range Π (robustness margin)
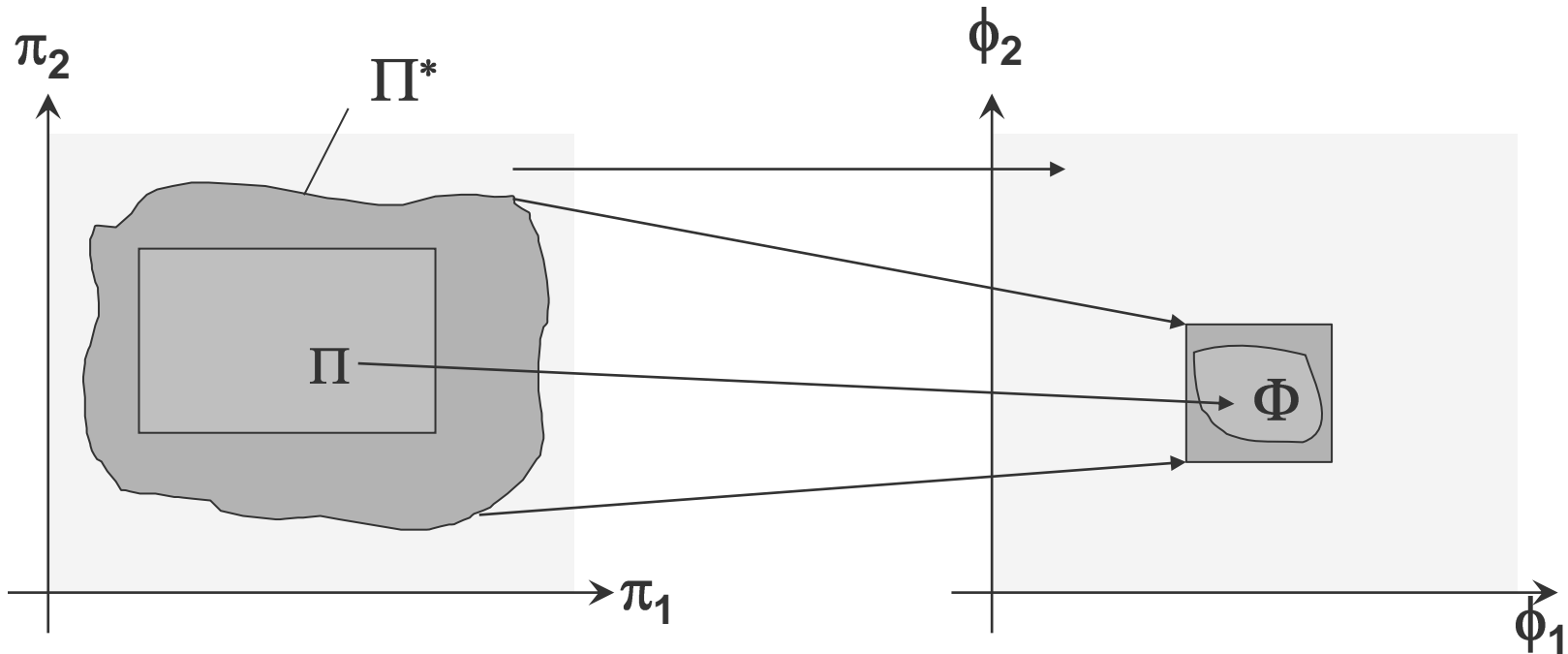
Specifies *against what* Φ of *f* is robust (operating conditions perturbation Π)

A non-robust design
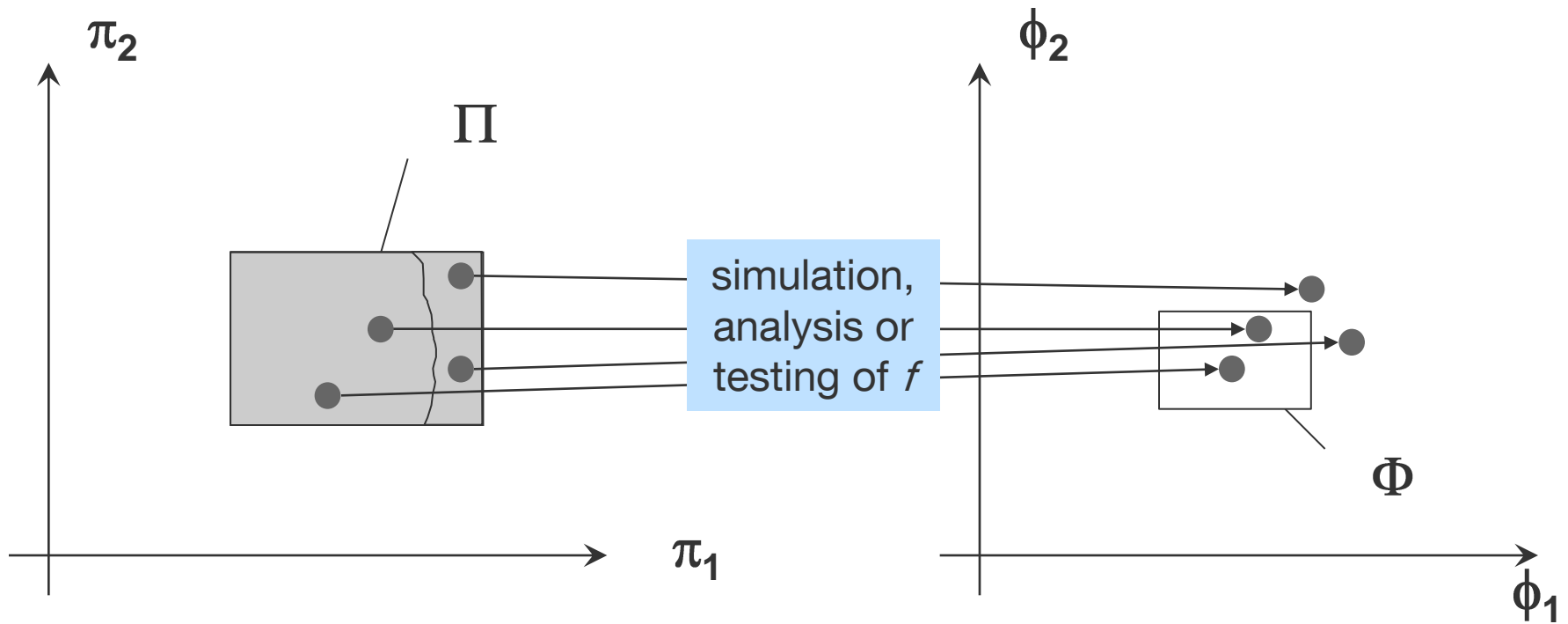
- $\pi \in \Pi$ exists so that $f(\pi) \notin \Phi$
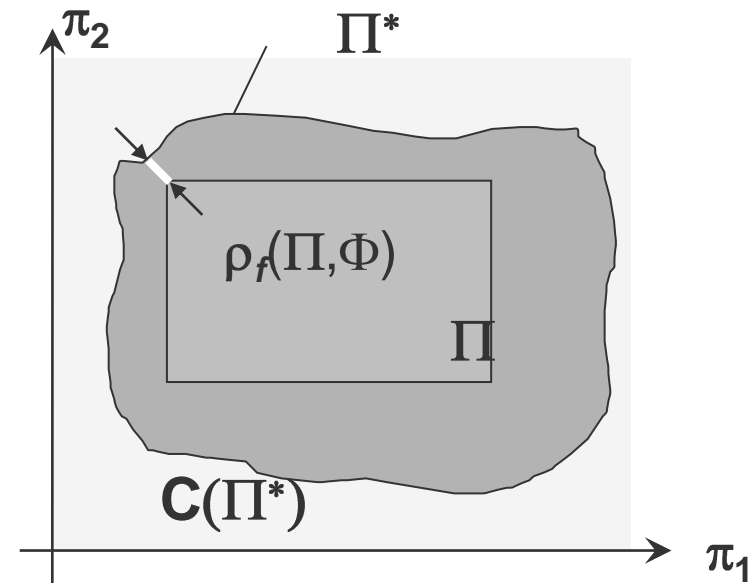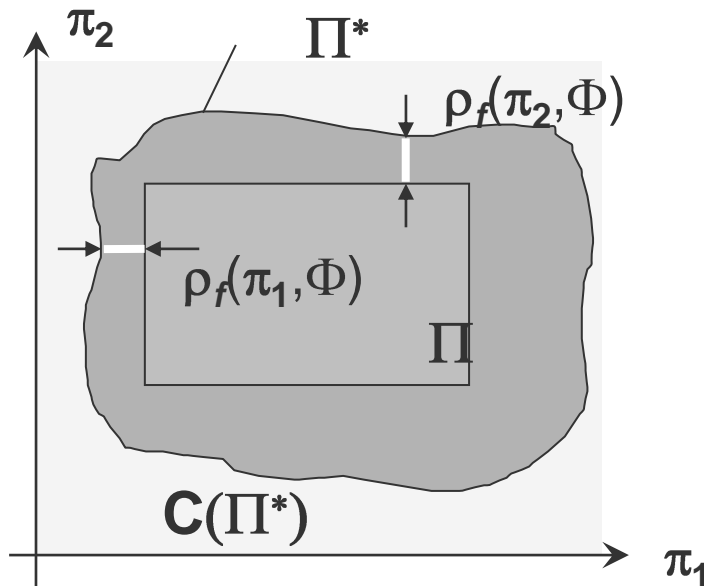- Robustness $\rho_f(\Pi, \Phi) = 0$

A robust design

- Robust closure Π^* so that $\Pi \subseteq \Pi^*$
- For all $\pi \in \Pi^* : f(\pi) \in \Phi$
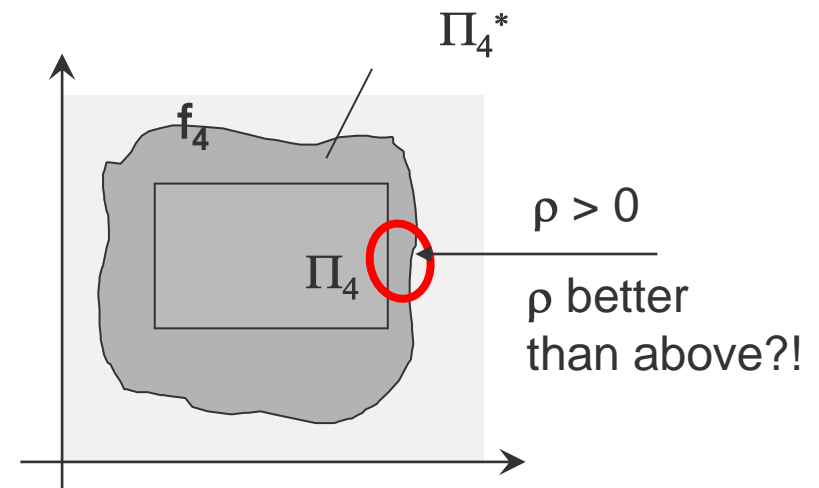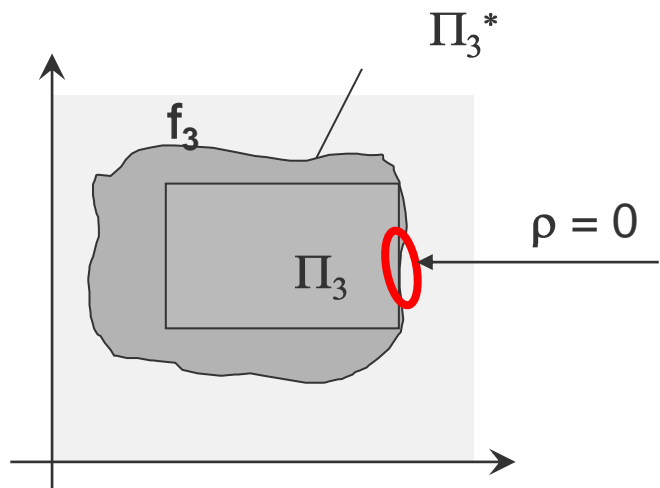- Robustness $\rho_f(\Pi, \Phi) > 0$

Whereas Π is specified,
Π^* is characteristic of the design

Quantifying robustness

- Robustness against π_i = min distance (1-dim) between points from $C(\Pi^*)$ and Π with identical coordinates except on axis *i*

- Global robustness = min distance (m-dim) between any two points from $C(\Pi^*)$ and Π, may be smaller than all ρ against π_i

Comparison of designs
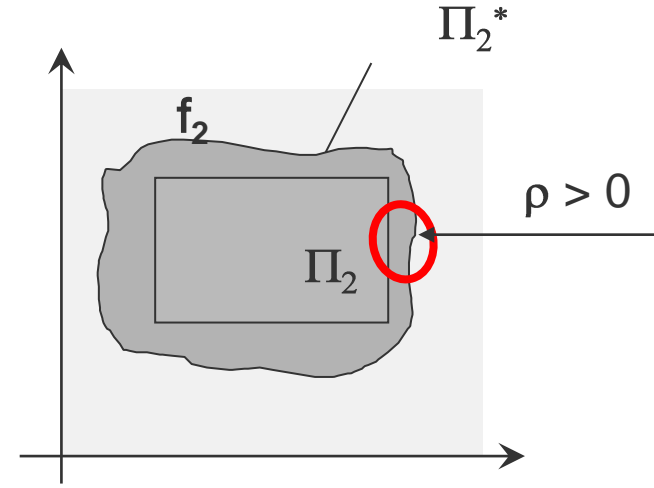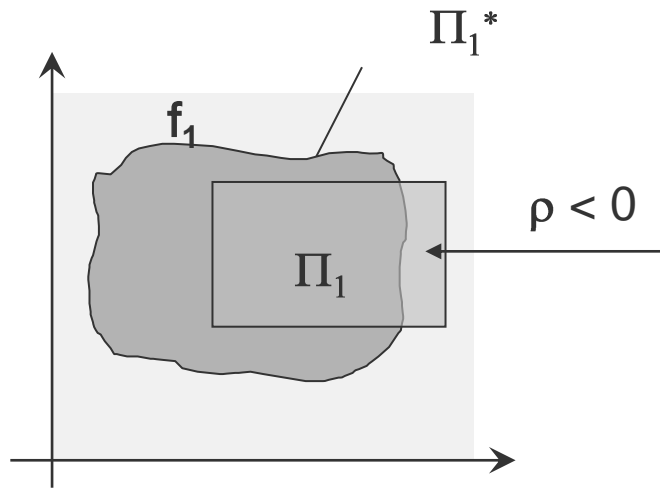
Π_1^*

f_1

$\rho < 0$

Π_1

Π_2^*

f_2

$\rho > 0$

Π_2

Π_3^*

f_3

$\rho = 0$

Π_3

Π_4^*

f_4

$\rho > 0$

Π_4

ρ better
than above?!

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  - Aging Monitors
- Robustness Validation (Martin Barke, Martin Radetzki)
  - Measuring robustness
  - **Robustness as a probability**
  - Robustness of Digital Circuits

Robustness as a probability

$$\Pi^* = f^{-1}(\Phi)$$

Robustness **R** is the conditional probability that a system works correctly, although it is operated outside the specification.*

$$\rho(\Pi, \Phi) = \Pr\{\vec{\phi} \in \Phi \mid \vec{\pi} \notin \Pi\}$$

$$= \frac{\int\limits_{\Pi^* \backslash \Pi} pdf_\pi(\vec{\pi}) d\vec{\pi}}{1 - \int\limits_\Pi pdf_\pi(\vec{\pi}) d\vec{\pi}}$$

Radetzki, M.; Bringmann, O.; Nebel, W.; Olbrich, M.; Salfelder, F.; Schlichtmann, U.: Robustheit nanoelektronischer Schaltungen und Systeme, 4. GMM/GI/ITG-Fachtagung Zuverlässigkeit und Entwurf, Wildbad Kreuth, September 2010.
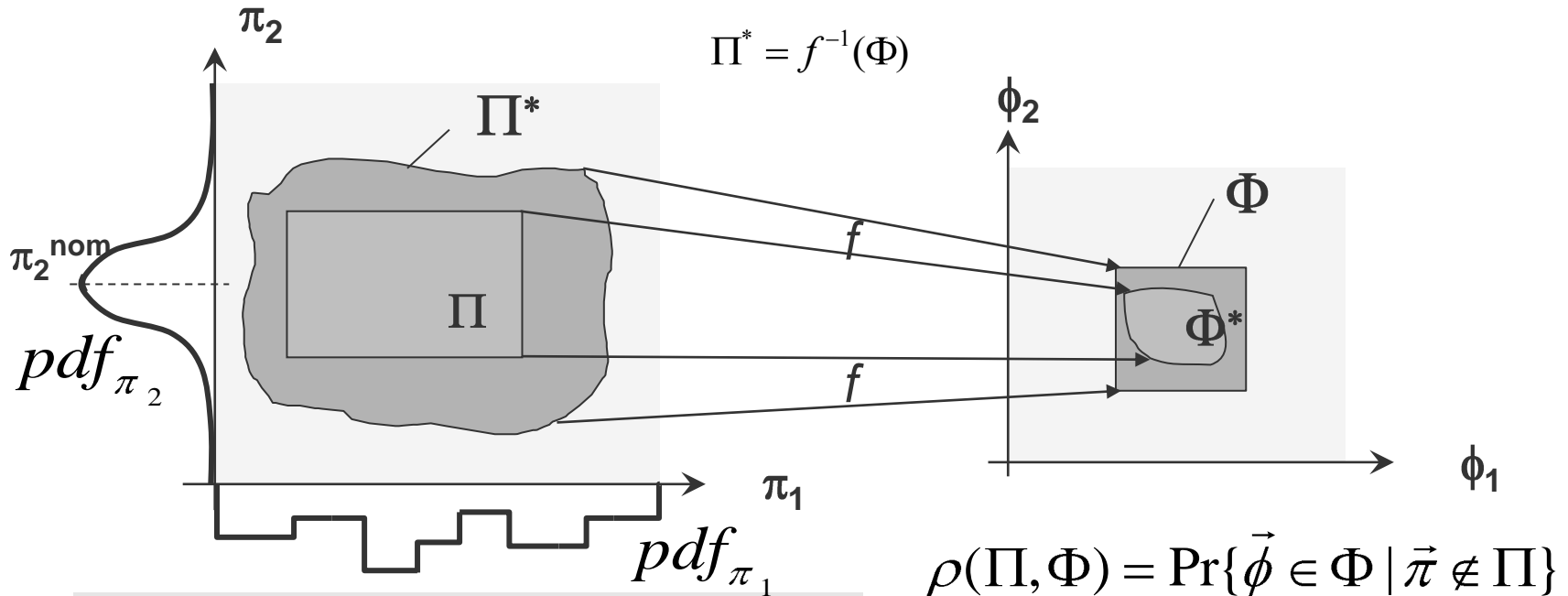
ROBUST

Agenda

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  - Measuring robustness
  - Robustness as a probability
  - **Robustness of Digital Circuits**

Robustness validation in the context of aging analysis

- Properties Φ: frequency **f**
- Operating conditions Π: temperature **T**, supply voltage $\mathbf{V_{dd}}$
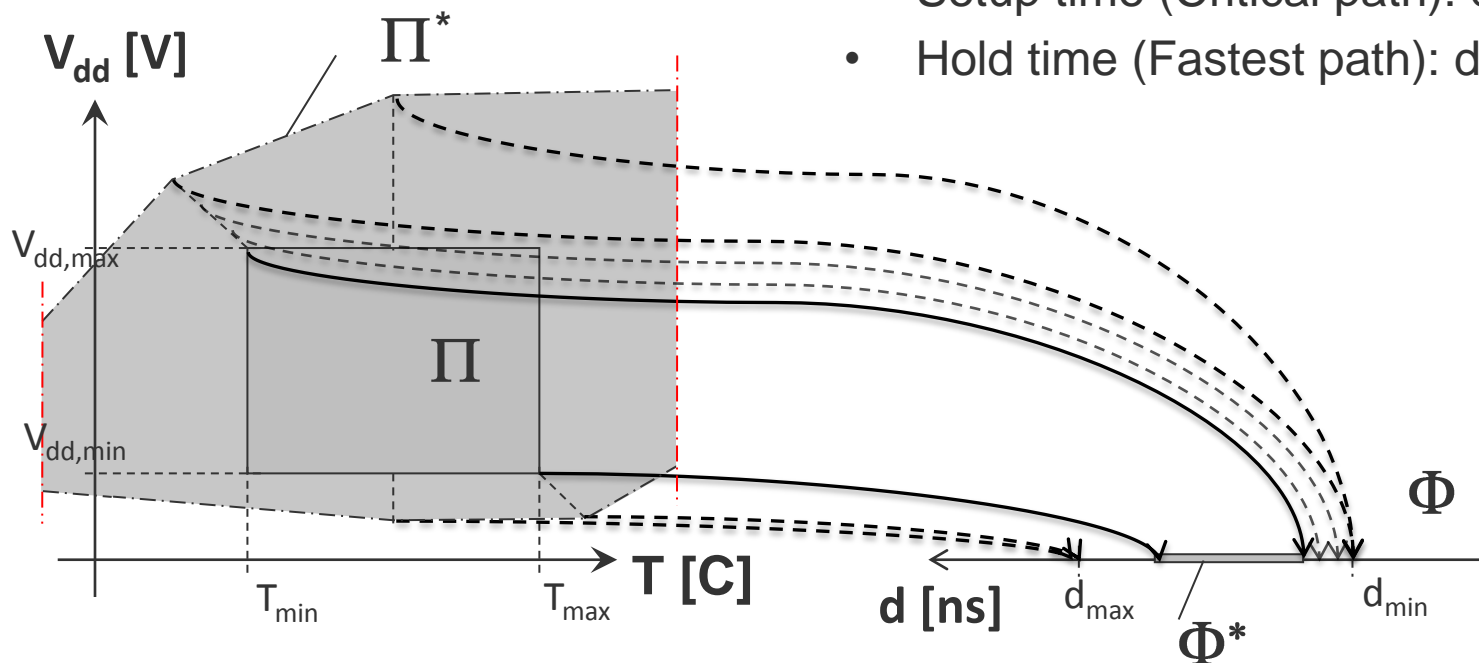
- Setup time (Critical path): d_{max}
- Hold time (Fastest path): d_{min}

Conclusion

- Sensitivity of IC circuits to parameter drifts increases with shrinking technologies -> This causes a reliability problem.

- Aged gate and RTL models:
    - Several possible critical paths must be considered during timing sign-off
    - High dependence on workload/operating conditions
    - Aging monitors one possibility to observe workload dependent aging effects

- Robustness
    - Evaluate circuits based on a mission profile that covers cases outside specified enviromental conditions.
    - Extended to include ageing degradation effects.